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Multi-rate Real Time Hybrid Simulation operated on a flexible LabVIEW real-time platform

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Abstract

This paper represents a real-time hybrid simulation (RTHS) strategy where the numerical and experimental substructures are executed at two different rates to optimize computational resources while maintaining good actuator control. The concept is referred to here as multi-rate real-time hybrid simulation (mrRTHS) which is operated on a Laboratory Virtual Engineering Workshop (LabVIEW) real-time target and demonstrated through a single and multiple degree-of-freedom (SDOF) and (MDOF) mass-spring-damper system. The numerical substructure generates a displacement signal with a coarse time step of Δt . Using the current and three previous displacement data points, a finer control signal is defined with a time step of δt , using a third order polynomial algorithm – referred to here as the polynomial fitting extrapolator. Both the numerical substructure and polynomial fitting extrapolator is executed with a sampling rate of Δt by an on-board single-core processor - referred to here as the digital signal processor (DSP). Through a field programmable gate array (FPGA) the control signal is compensated and transmitted to the transfer system through an I/O module with a sampling rate of 1 kHz (i.e. $\delta t = 0.001\text{sec}$). The ratio between Δt and δt are an integer - referred to here as the execution ratio. For an execution ratio of 1:5 and 1:10 the system performance is evaluated against a numerical model of the emulated structure – referred to here as the reference. For the SDOF system, a root-mean-square (RMS) error of 7.45% and 7.67% is identified between the mrRTHS and reference for an execution ratio of 1:5 and 1:10 respectively. For the MDOF system, a RMS error of 2.50% and 5.41% is obtained. When changing the execution ratio from 1:5 to 1:10 an approximately 50% reduction of the required computational resources on the DSP is achieved.

Keywords: *Real-time hybrid simulation, hardware-in-the-loop, performance evaluation, experimental substructure, numerical substructure, field programmable gate array*

1. Introduction

Hybrid simulation is a substructuring technique where a structure of interest is emulated by combining the advantages of numerical modeling with those of experimental testing [1], [2]. Here, the numerical substructure typically includes the majority of the emulated structure which represents either predictable mechanical behavior or is considered uncritical for the analysis conducted. The remainder of the emulated structure is of special interest and is for that reason physically replicated to reveal the effects of e.g. viscoelasticity, buckling, rate dependent properties or other non-linear effects. As a consequence, neither cost-intensive full-scale experiments nor demanding theoretical evaluation procedures are required to reveal the response of the emulated structure [3], [4]. The coupling governed through the interface between the numerical and experimental substructure – referred to here as the shared boundary - is achieved by maintaining compatibility and equilibrium at the interface. During the test, a predefined external load is applied the numerical substructure and the corresponding response computed. Through a communication loop, the displacement at the shared boundary is acquired and applied to the experimental substructure through a servo-hydraulic transfer system. The forces required to meet the boundary conditions between the numerical and experimental subassemblies – referred to here as the restoring force – are fed back to the numerical substructure to reveal the response of the emulated structure. The experimental and numerical substructure, communication loop and servo-hydraulic transfer system is combined to form the hybrid simulation.

The research within hybrid simulation has primary been focusing on testing of seismic protection of building structures on either a real-time or extended time-scale [5], [6], [7], [8]. Here, the shared boundary between the numerical and experimental substructure typically consists of a set of discrete points with a few degrees-of-freedom (dofs) referred to here as multi-component hybrid simulation. For this application, the load bearing structure is simulated in a numerical model while damping fixtures are tested experimentally including: elastomer [9], stud types [10], [11] and magneto-rheological [12], [13], [14]. However, multi-component hybrid simulation is becoming a mature, reliable technology, which opens the opportunity to spread the hybrid simulation technique to other application areas including: large-scale composite structures [15].

1 The ambition to improve the structural and operational performance in the wind energy industry [16] has resulted in
2 extensive research within large-scale and high performance composite structures. In these efforts, testing has primary
3 been focusing on two scales: full scale and coupon material testing [17]. Full scale testing provides valuable knowledge
4 of the structural behavior; however it requires large laboratory facilities and typically entails significant simplifications
5 of the load configurations applied, compared to the actual loads to which the structure is exposed during service. On
6 the other hand, material characteristics are normally provided through small scale testing performed on specially
7 designed standardized specimens. This approach does not require large laboratory facilities; however it introduces
8 idealized stress and strain states in the test specimens and as a consequence, does not account for the material
9 behavior under complex stress states and interactions between the different materials and joints, bearings and other
10 critical details throughout the structure.
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14 To address shortcomings in full scale and material testing, the hybrid simulation concept is implemented for large
15 scale composite structures – referred to here as single component hybrid simulation. Single component hybrid
16 simulation is a substructuring technique, capable of evaluating the global response of the emulated structure under
17 the influence of local effects and when exposed to advanced load configurations [18]. However the single component
18 hybrid simulation technique highly complicates the numerical and experimental substructure due to the complex
19 geometry and material characterization. Furthermore, the shared boundary is continuous along the edge which leads
20 to transferring of response in – ideally – an infinite number of contact points, potentially yielding a complex
21 force/displacement distribution in the coupling between the two substructures. Previous research has been carried
22 out within the field of single component hybrid testing on a composite structure with the shared boundary covering; a
23 single discrete point with multiple and single axis control [18], [19]. However, both studies only cover the quasi-static
24 regime the relevance of which is somewhat limited given that the significance of structural dynamics is becoming
25 increasingly important as lighter, cheaper, higher and larger structures become more frequent. As a consequence,
26 static testing and analysis have only limited relevance for structures exposed to dynamic loads including wind,
27 earthquake, traffic from vehicles and pedestrians, etc.
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32 Real time hybrid simulation (RTHS) is a useful technique to evaluate the performance of structural dynamics [20].
33 Roughly, the RTHS communication loop can be separated in to two tasks including solving the numerical substructure
34 and operating the shared boundary. Due to the inherent dynamics in the experimental substructure, the shared
35 boundary needs to follow a continuous time history of displacement, velocity or acceleration with a frequency of
36 operation which is 10-25 times higher than the mode of interest [21]. In conventional RTHS the numerical
37 substructure and shared boundary is operated sequentially at an identical rate. However, given the increased
38 complexity of the numerical substructure within single component hybrid simulation, this execution frequency can be
39 difficult to achieve with the available onboard computational resources due to the implementation of e.g. non-linear
40 effects along with numerous degrees of freedom. Furthermore, the use of commercial FE-software could be of
41 interest [18], [19] which may require access through a network to a remote computer. For all these reasons, the
42 numerical substructure may require an extended integration time, compromising the ability to represent the
43 underlying dynamics of the system. To optimize available computational resources and enhance flexibility to the RTHS
44 architecture, the numerical substructure and shared boundary are executed at two different rates – referred to here
45 as multi-rate real-time hybrid simulation (mrRTHS).
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51 The mrRTHS strategy has been presented previously in the literature by [8], [22]. Here, both the numerical
52 substructure and shared boundary are handled through a single core processor using the programming language C.
53 Other platforms capable of handling e.g. Matlab commands exist; however the C language provides the most
54 computationally efficient approach. Continuous real-time loading of the shared boundary is provided through a
55 combined extrapolation and interpolation procedure, inducing a communication delay equivalent to the integration
56 time of the numerical substructure. Furthermore, an irregular step is identified between the last extrapolated points
57 and consecutive interpolated one, as discussed in [23]. Alternatives to the mrRTHS exist including parallel real-time
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1 computing techniques [24]. This parallelization of the real-time system enables higher simulation frequency of the
2 numerical model by allowing multiple threads to execute simultaneously across multiple processors [25].
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4 The scope of this paper is to implement and demonstrate an mrRTHS strategy to extend the boundaries of existing
5 RTHS systems by optimizing the computational resources. This strategy is operated through a Laboratory Virtual
6 Engineering Workshop (LabVIEW) real-time target capable of providing deterministic and real-time performance for
7 data acquisition and control systems. The numerical substructure is discretized through an explicit state-space
8 representation with a coarse time step of Δt . By the current and 3 previous displacement data points, a finer control
9 signal is generated with a time step of δt , using a third order polynomial algorithm – referred to here as the
10 polynomial fitting extrapolator. Both the numerical substructure and polynomial fitting extrapolator is executed with a
11 sampling rate of Δt by an on-board single-core processor – referred to here as the digital signal processor (DSP).
12 Through a field programmable gate array (FPGA) the control signal is compensated through a feedforward (FF)
13 compensator and transmitted to the transfer system through an I/O module with a time step of δt . Thus the tasks
14 related to the numerical substructure and shared boundary is dedicated its own processor to allocate computationally
15 independent and separated resources. The ratio between Δt and δt is an integer - referred to here as the execution
16 ratio. The mrRTHS strategy is demonstrated through a single and multiple degree-of-freedom (SDOF) and (MDOF)
17 mass-spring-damper system in order to reduce the complexity in verifying the software capabilities when handling the
18 test response and theory. The system characterization is identified and a suitable delay compensation scheme
19 implemented to account for communication delay and dynamics in the transfer system. The mrRTHS communication
20 loop is tested and verified against a numerical model of the emulated structure – referred to here as the reference.
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26 **2. mrRTHS communication loop**

27 **2.1. Configuration for mrRTHS**

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29 The overall architecture of the mrRTHS communication loop includes a transfer system and two loops named main-
30 and outer-loop, which are handled in a producer/consumer configuration [26]. The outline of the dataflow in the
31 mrRTHS communication loop is separated in 9 units labeled from **(1)** to **(9)** presented in Figure 1.
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35 The mrRTHS communication loop is operated through a CompactRIO 9074 (cRIO – 9074) [27] including the FPGA and
36 400MHz onboard single-core processor – referred to here as the Digital Signal Processor (DSP). The FPGA offers high
37 reliability and determinism given that all logics are compiled to the physical hardware, and for that reason, does not
38 utilize any overarching operating systems. However, this comes with the tradeoff of having a relatively small amount
39 of memory available on the FPGA, implying a limited complexity of the on-board algorithm. The interface between the
40 mrRTHS communication loop and transfer system is handled through a digital to analog (NI9263) [28] and analog to
41 digital (NI9205) [29] I/O module. The cRIO – 9074 and I/O modules combine to form the real time target.
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45 The main-loop is operated through the DSP with a coarse time step of Δt . Here the numerical substructure in **(1)**
46 computes the next step displacement signal $d_{num}(t)$ based on the external load and last available restoring force $F_{res}(t-$
47 $i)$. Through the current and previous data points provided by **(1)**, the predicted system response after the
48 communication delay is identified as the displacement signal $d_{pred}(t)$ in **(2)**. Between each data point provided by **(2)**
49 the displacement signal is resampled through extrapolation $d_{exp}(t+i)$ in **(3)** with the time increment δt for $i \in [0; \Delta t]$.
50 The delay compensation in **(2)** and polynomial fitting extrapolator in **(3)** are both handled by a 3rd order polynomial
51 algorithm, further described in section 3.2.
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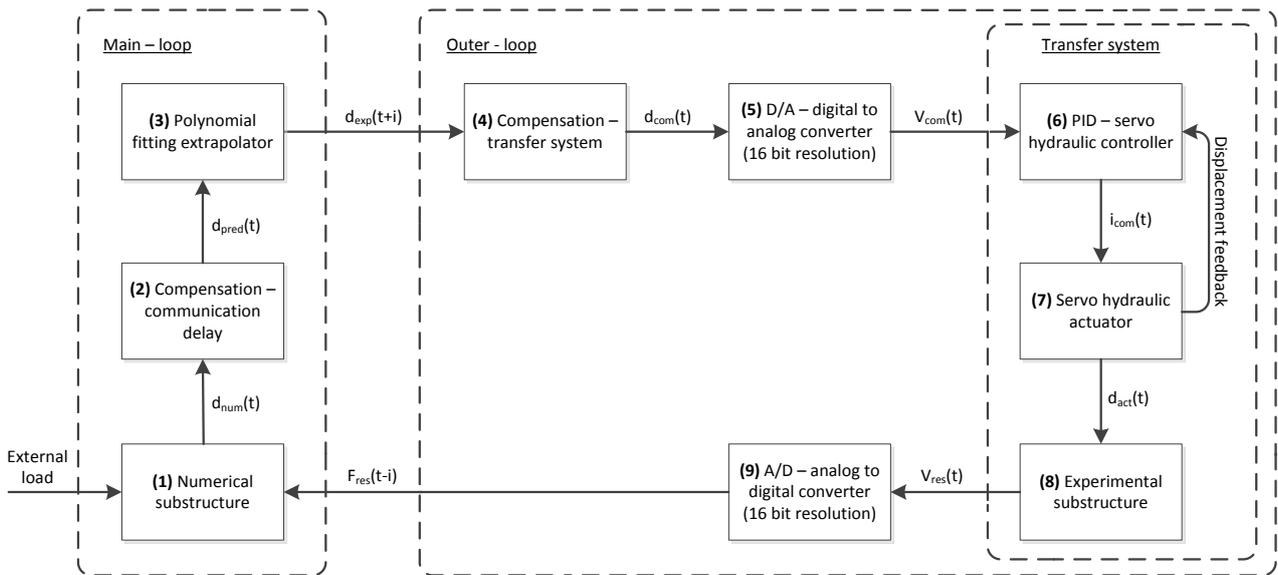


Figure 1: Schematic block diagram representing the overall architecture for the mrRTHS communication loop

The outer-loop is operated through the FPGA with an execution rate of 1 kHz (i.e. $\delta t = 0.001\text{sec}$) allowing the shared boundary to handle frequencies of up to 100 Hz [21]. Here the actuator displacement after the delay/lags, associated with the dynamics of the transfer system, is predicted to generate the command displacement $d_{com}(t)$ through a FF compensator in (4). Further details of the FF compensator in (4) are given in section 3.1. From the data points provided by (4) an equivalent DC voltage $V_{com}(t)$ is generated in (5) to operate the transfer system. The corresponding restoring force $V_{res}(t)$ are acquired from the transfer system and converted to a digital signal in (9).

The transfer system is operated by transmitting the real-time command signal $V_{com}(t)$ to a digital proportional-integral-derivative (PID) controller model: Shore Western SC6000 in (6). To prevent data loss due to under sampling, the execution rate of the transfer system F_{PID} is set equal to or higher than the outer-loop (i.e. $1\text{ kHz} \leq F_{PID}$). Through the PID controller, an electrical current $i_{com}(t)$ is generated to operate a Schenck-Pegasus 162M servo-valve with a capacity of 15 GPM at 3000psi in (7). The servo valve is connected to a Shore Western 910D-77-6-4-348 actuator with a 6.0 inch stroke and 1.1kip force capacity. The actuator displacement $d_{act}(t)$ is measured through an internal LVDT model: G.L Collins, LMT-711P34 and the associated restoring force monitored by a Omega S-beam load cell model: LCM101-2K (S/N 245518) with a capacity of ± 2 kips. The experimental substructure in (8) consists of a spring with the stiffness k_e , further defined in Table 1. The standard uncertainty of the repeatability offered by the transfer system is given by: $3.33 \cdot 10^{-4}$ inch and 1.53lbs. The repeatability is identified from a sample of 100000 measurements, acquired under constant conditions with a sampling frequency of 1 kHz.

2.2. Communication interface between main- and outer-loop

The interface between the main- and outer-loop is handled through a dual channel Direct Memory Access (DMA) First-In-First-Out (FIFO) configuration [30]. Here the data received from the extrapolator algorithm in (3) and restoring force in (9) is buffered and exchanged between the two loops cf. Figure 1. A schematic of the main- and outer-loop switching logic are outlined in Figure 2, separated in an initiating, running and completion sequence. The initiating and completion sequence represents the first and last main-loop time step respectively. The running sequence represents the switching logic for the remaining duration of the mrRTHS. For demonstration purposes, only a couple of main-loop time steps are represented cf. Figure 2.

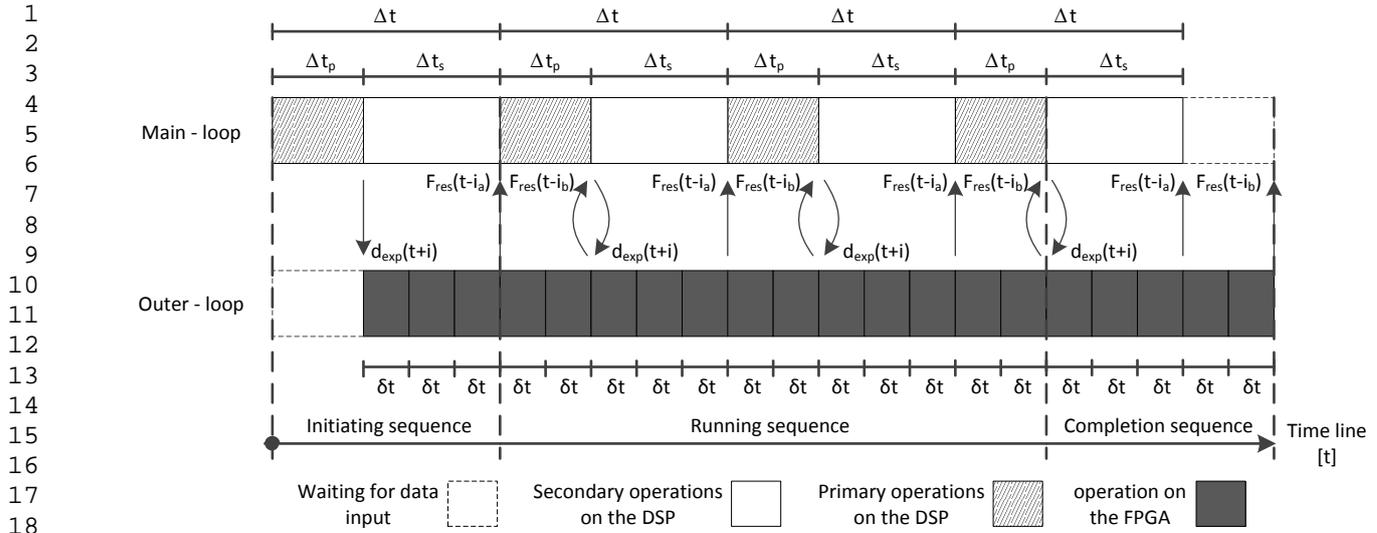


Figure 2: Schematic of the main- and outer-loop switching logic for an execution ratio of 1:5

The numerical substructure, communication delay compensator and extrapolated displacement signal $d_{\text{exp}}(t+i)$ are computed in the main-loop through primary operations for the duration of Δt_p and buffered in the DMA FIFO. When the primary operations of the DSP are completed, the secondary tasks include: file manipulation, TCP/IP communication, etc. is handled for the duration of Δt_s . The total time step of the main loop Δt is identified as the sum of Δt_p and Δt_s cf. Figure 2. In parallel the FPGA is emptying and processing the received displacement signal while buffering the corresponding restoring force $F_{\text{res}}(t-i)$ in the DMA FIFO with a time increment of δt for $i \in [0; \Delta t]$. Given that $\Delta t_p > 0$, a communication delay is included given that only $F_{\text{res}}(t-i_a)$ for $i_a \in [\Delta t_p; \Delta t]$ is available in the DMA FIFO when the next displacement signal is computed. While the primary operation in the main-loop is completing, the remaining restoring forces $F_{\text{res}}(t-i_b)$ in the DMA FIFO for $i_b \in [0; \Delta t_p]$ is acquired and the next extrapolated displacement signal $d_{\text{ext}}(t+i)$ returned for the upcoming main-loop iteration. The duration of Δt_p is regulated by the available computational resources of the DSP and the complexity of the primary operations in the main-loop algorithm. The switching logic for the main- and outer-loop The initiating sequence executes the numerical substructure on the basis on predefined initial conditions the mrRTHS communication loop is initiated by running the

2.3. Implementation/design of the control platform

The main framework for the mrRTHS platform is divided into 5 units labeled from **(1)** to **(5)** in Figure 3. Here, the host application in **(1)** operates the user interface along with data storage and external load. This is done through a master computer (personal computer) which typically comprises ample onboard memory and computational resources. Through a TCP/IP communication, the master computer continuously transmits the predefined external load and user defined inputs, while receiving feedback to and from **(2)** in the main-loop. This configuration is required due to the limited on-board memory available on the cRIO – 9074.

The main-loop is divided into a secondary **(2)** and primary **(3)** portion, both operated by the DSP as outlined in Figure 3. The interface between **(2)** and **(3)** are provided through a producer/consumer configuration [26], where **(2)** consists of two separate while loops: a) producer loop that transmits the feedback data to **(1)** and b) consumer loop that receives the external load from **(1)**. The primary operation by **(3)** is handled through a single while loop which both transmits the feedback data and receive the external load to and from **(2)**. To reduce jittering and optimize the computational resources of the DSP, each of the three while loops in the main-loop are assigned the following order of priority: a) deterministic loop in **(3)**, b) consumer loop in **(2)** and c) producer loop in **(2)**. By prioritizing each task, it is ensured that the secondary operations in **(2)** are halted whenever computational resources are needed for primary operations in **(3)**. Furthermore, the flow of external load is prioritized ahead of feedback data.

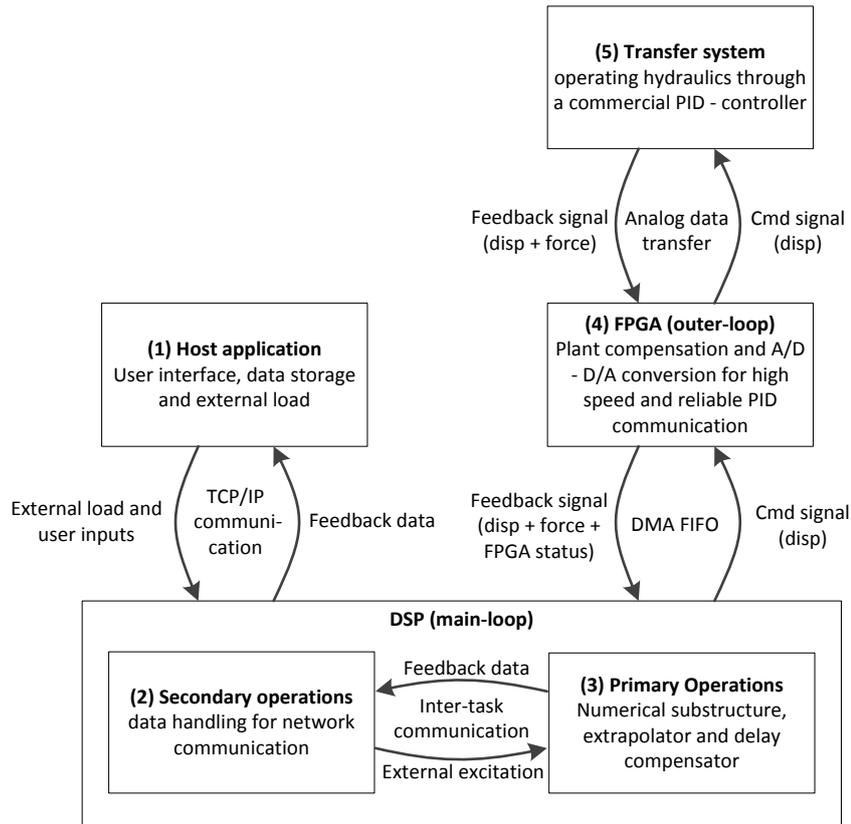


Figure 3: The main framework of the mrRTHS software

The outer-loop is handled in (4) operated by the FPGA as outlined in Figure 3. Here the interface between the main-loop and outer-loop is established through the DMA FIFO as clarified in section 2.2. The displacement signal from the numerical model is transmitted from (3) to (4) for further processing and the feedback signal returned for monitoring of the system response. Given the fast execution rate and high reliability of the FPGA, interlocks are here implemented to prevent damage to the transfer system and its surroundings. The transfer system is operated through the I/O modules which offer a high speed and reliable analogue data transfer. Here the displacement signal is transmitted from (4) to (5) and corresponding feedback data received including measured displacement and restoring force.

3. System characterization

3.1. Actuator dynamics

The dynamics of the entire transfer system including servo-hydraulic actuator, PID controller and experimental substructure, represent a significant source of time delay/lags in the RTHS communication loop [4]. Thus, compensation is crucial to ensure accuracy and stability of the RTHS [31]. To understand the system behavior in a wide range of frequencies and amplitudes, open loop system identification is performed through a band-limited white noise with a frequency ranging from 0 to 15Hz and a root-mean-square (RMS) of 0.01 inch. Based on an obtained data series of 300000 measurements, acquired with a sampling rate of 1 kHz, the system identification in the frequency domain are given in Figure 4.

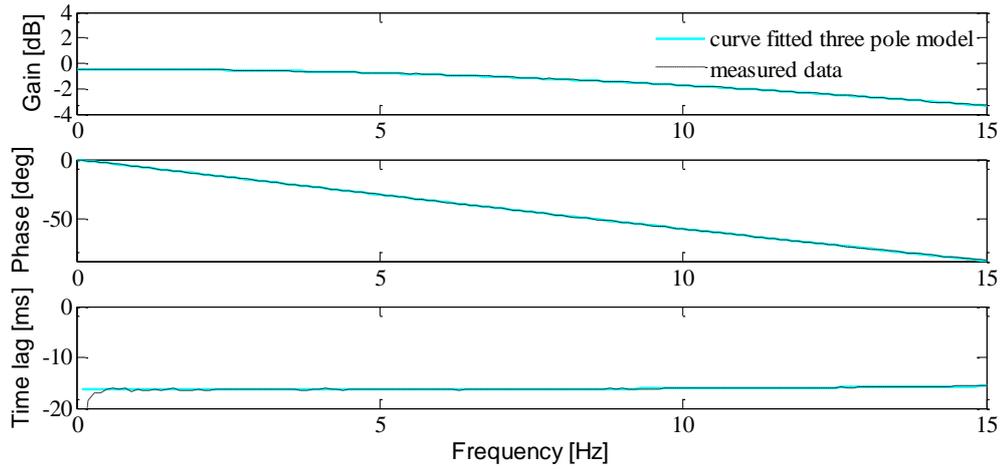


Figure 4: System identification in the frequency domain - open loop transfer function

The magnitude is demonstrating an undershooting in the entire bandwidth, which is nearly constant in the range: 0-4Hz. In the remaining frequency domain, the magnitude starts to roll off as a function of the frequency. The phase of the dynamic system is nearly linear throughout the entire bandwidth, resulting in a constant time lag of approximately 16.4ms. A three pole model is found sufficient to accurately represent the dynamics over the entire frequency range: 0-15Hz cf. Figure 4. The curve fitted continuous transfer function $G_a(s)$ is presented in the frequency domain s in eq. (1).

$$G_a(s) = \frac{5.163 \cdot 10^6}{s^3 + 530.8s^2 + 8.899 \cdot 10^4 s + 5.44 \cdot 10^6} \quad (1)$$

To cancel the dynamics of the transfer system over the frequency range of interest, a FF compensator is implemented [32]. For an SDOF system where only a single eigenfrequency of 1.00Hz is present cf. Table 1, a direct inverted first order compensator is deemed sufficient. The discrete first order direct inverted compensator $K_a(z)$ is presented in the z -domain by eq. (2).

$$K_a(z) = \frac{\alpha z - (\alpha - 1)}{z} \quad (2)$$

Here α is calibrated so that the measured and desired displacement correlate in the frequency range of interest. This calibration process is conducted through an open loop sinusoidal reference signal. For the MDOF system the eigenfrequency ranges from 1.77 – 7.71Hz cf. Table 1, meaning that a higher order transfer function is required to ensure good performance in the entire frequency range of interest. Given that a three pole model accurately represents the dynamics of the transfer system cf. Figure 4, a discrete third order inverted compensator [33] is implemented in the time domain t - presented by eq. (3).

$$K_a(t) = a_0 r(t) + a_1 \dot{r}(t) + a_2 \ddot{r}(t) + a_3 \dddot{r}(t) \quad (3)$$

Here, the coefficients a_0 through a_3 are given by eq. (1) and the dots denote differentiation of the desired displacement r with respect to time t . The closed loop performance of the first and third order compensators is outlined in Figure 10 and 12, respectively.

3.2. Communication delay and extrapolation

Both communication delay and extrapolation are handled through an algorithm capable of predicting the desired displacement. Various forward prediction schemes have been investigated for the use in mrRTHS [24]. In this study,

the polynomial fitting extrapolator (third order polynomial algorithm) is selected for further analysis due to the minimal computational resources needed to run the algorithm, making it well suited for real time analysis. By the use of the current and 3 previous data points provided with a time step of ΔT , the control signal is extrapolated with a predefined time step t in eq. (4).

$$d_{exp} = \sum_{i=0}^N a_i d_i \quad (4)$$

Here N , d_i and a_i represent the order of the algorithm (i.e. $N = 3$), the current and 3 previous data points with the time step ΔT , and polynomial coefficients generated through the Lagrange formula, respectively. For a fully independent relation between t and ΔT , the polynomial coefficients a_i are given by eq. (5) – (8) cf. [23].

$$a_0 = \frac{t}{\Delta T} \left(\frac{11}{6} + \frac{t}{\Delta T} + \frac{1}{6} \left(\frac{t}{\Delta T} \right)^2 \right) \quad (5)$$

$$a_1 = -\frac{t}{\Delta T} \left(3 + \frac{5}{2} \frac{t}{\Delta T} + \frac{1}{2} \left(\frac{t}{\Delta T} \right)^2 \right) \quad (6)$$

$$a_2 = \frac{t}{\Delta T} \left(\frac{3}{2} + 2 \frac{t}{\Delta T} + \frac{1}{2} \left(\frac{t}{\Delta T} \right)^2 \right) \quad (7)$$

$$a_3 = -\frac{t}{\Delta T} \left(\frac{1}{3} + \frac{1}{2} \frac{t}{\Delta T} + \frac{1}{6} \left(\frac{t}{\Delta T} \right)^2 \right) \quad (8)$$

Compensation of the communication delay $d_{pred}(t)$ is achieved for $t = \Delta t_p$ cf. Figure 2. Here, d_i is the current and 3 previous data points provided by the numerical substructure $d_{num}(t)$. The extrapolated displacement signal $d_{exp}(t+i)$ is generated with a time step of $t = \delta t$ for $i \in [0; \Delta t]$ and d_i the current and 3 previous data points provided by $d_{pred}(t)$.

The performance of the polynomial fitting extrapolator is investigated through a chirp sinusoidal wave with a linearly increasing frequency ranging from 0 to 10 Hz for the duration of 10 seconds and constant amplitude of 0.15 inch. The signal is generated with two different sampling rates including: 100Hz and 1 kHz named under sampled and desired signal respectively. With an execution ratio of 1:10, the under sampled signal is resampled through extrapolation $d_{exp}(t)$ and compared with the desired signal – referred to here as desired cf. Figure 5.

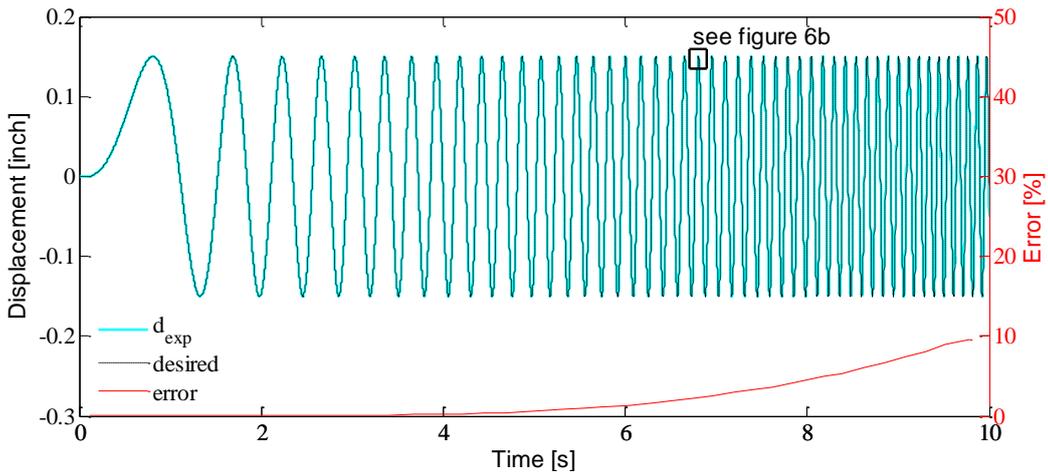


Figure 5: Extrapolation performance with a chirped sine wave in the domain 0-10Hz and execution ratio 1:10

Here the error is presented as the relative deviation between the extrapolated $d_{exp}(t)$ and desired signal cf. eq. (9). To smooth the presented error output, only the peak error within each displacement period is presented.

$$Error(t) = \frac{|d_{exp}(t) - desired(t)|}{\max(|desired(t)|)} \cdot 100 \quad (9)$$

The same approach is used for other execution ratios, and the corresponding error presented in Figure 6a. From Figure 5 and 6a the error between the extrapolated and desired signal is related to the execution ratio and frequency (acceleration). In Figure 6b, a detail of the desired signal and corresponding extrapolated signal is presented. Here, the error between the extrapolated and desired signal is gradually increasing as a function of time. For that reason, an irregular step (discontinuity) is bound to happen between the last extrapolated point $d_{exp}(t)$ and consecutive displacement signal $d_{pred}(t)$.

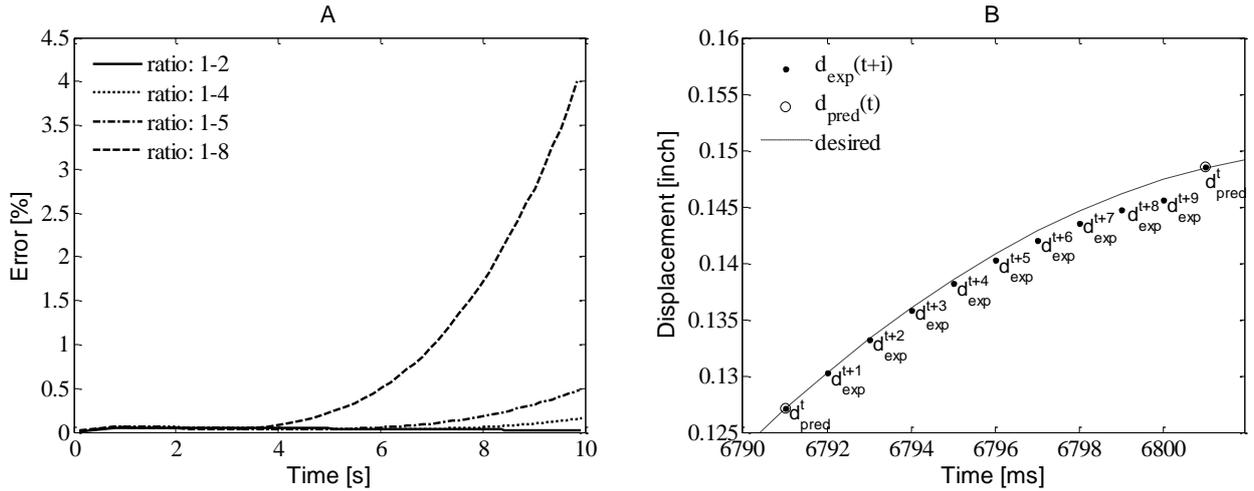


Figure 6: chirped sine wave in the domain 0 – 10hz: a) error between the desired and extrapolated signal and b) correlation details

Increasing the order of the polynomial fitting extrapolator improves the performance in the higher frequency domain; however this comes with the trade-off of increased: a) vulnerability to system noise and b) required computational resources. Thus, we chose not to increase the order of the polynomial any further.

4. Emulated structure and shared boundary

The emulated structure consists of an SDOF and MDOF mass-spring-damper system loaded by the external load g_{acc} cf. Figure 7a and 7b. The spring stiffness k_e is represented as the experimental substructure while the remainder of the emulated structure is discretized through an explicit state-space representation. The shared boundary is further clarified in Figure 7c.

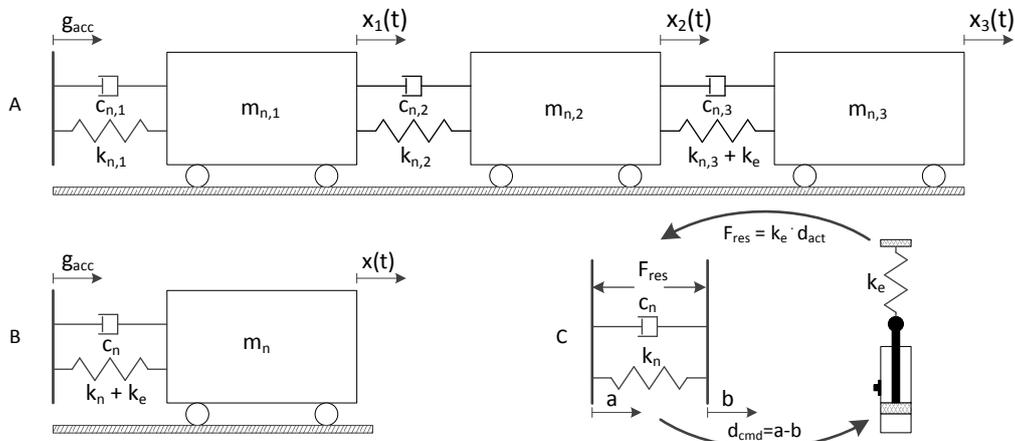


Figure 7: Schematic of the emulated structure and shared boundary: a) MDOF system, b) SDOF system and c) details of the shared boundary

To conduct a successful mrRTHS, global stability and performance are the major issues. In [34] and [35], predictive stability and performance indicators (PSI and PPI) have been developed to assess the sensitivity of an RTHS configuration to any phase discrepancy at the shared boundary resulting from transfer system dynamics and computation/communication delays. These metrics predict how transfer system dynamics and computation/communication delays, which are significant sources of systematic experimental error in RTHS, distort RTHS responses and how the corresponding error propagates through the entire simulation and may de-stabilize the system. Thus, PPI and PSI are used here to design a successful RTHS configuration from a stability and performance perspectives. Using PSI and PPI, the design of a successful RTHS is provided in Figure 8. On the basis of the PSI and PPI indicators outlined in Figure 8, SDOF and MDOF mrRTHS configurations are defined as presented in Table 1.

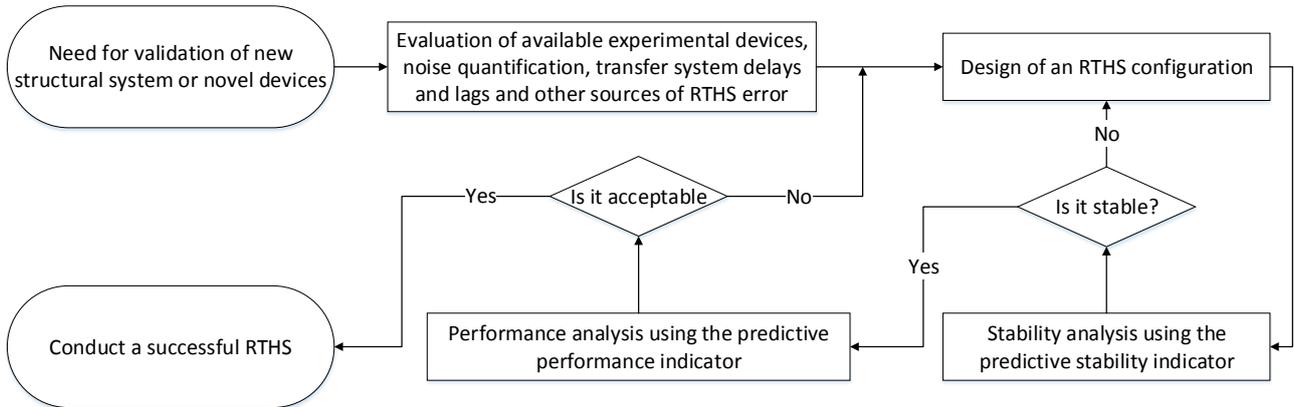


Figure 8: Design flow of a successful real-time hybrid simulation

Structure [-]	Module [-]	m_n [kg]	c_n [N'sec/m]	k_n [kN/m]	k_e [kN/m]	Mode [-]	Modal period [Hz]	Mode damping [%]
MDOF	1	440	880	275	-	1	1.77	1.78
	2	440	880	275	-	2	4.96	4.99
	3	440	880	165	110	3	7.17	7.21
SDOF	1	6300	2370	110	110	1	1.00	2.99

Table 1: Structural parameters of the numerical and experimental substructure for the mrRTHS

5. Test results

The mass-spring-damper systems are tested in SDOF and MDOF configurations for the duration of 70 sec. Here the mrRTHS architecture is evaluated using the normalized relative error between the mrRTHS and reference presented in eq. (10).

$$Error(t) = \frac{|mrRTHS(t) - REF(t)|}{\max(|REF(t)|)} \cdot 100 \quad (10)$$

The system is loaded by the Chichi earthquake – referred to here as the external load g_{acc} . The external load is showed in Figure 9 for both the SDOF and MDOF mrRTHS. The magnitude of the load is adjusted to achieve a maximum displacement of the shared boundary of approximately 0.15 inch.

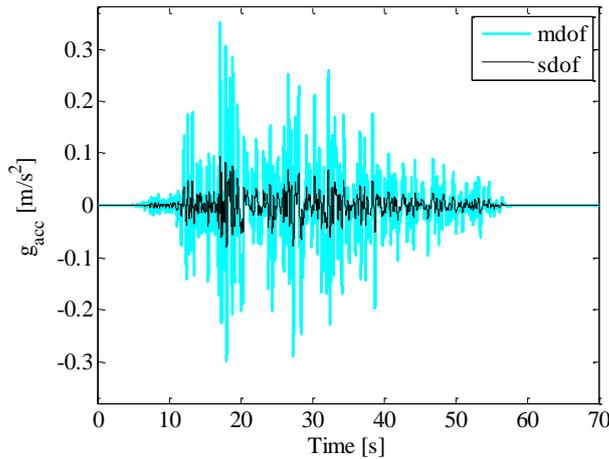
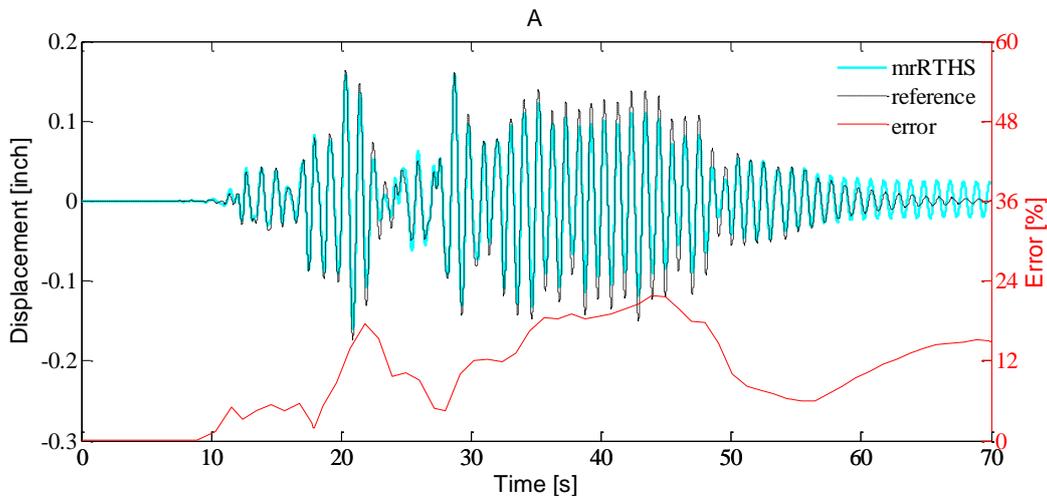


Figure 9: Chichi earthquake applied on the SDOF and MDOF system

The stiffness ratio between k_n and k_e at the shared boundary is set to 50% and 66% for the SDOF and MDOF configurations, respectively cf. Table 1. The performance of the mrRTHS architecture is demonstrated in both cases for an execution ratio of 1:5 and 1:10 with the outer loop running at a constant rate of 1kHz (i.e. $\delta t = 0.001\text{sec}$).

5.1. SDOF mrRTHS

For the SDOF mass-spring-damper system, the relative displacement $x(t)$ (see Figure 7b) is presented for the mrRTHS and reference for an execution ratio of 1:5 and 1:10 in Figure 10. The corresponding relatively error between the mrRTHS and reference are determined cf. eq. 10. The time step of the primary operation of the main loop Δt_p is 1ms. The computational complexity of the main-loop causes the DSP to operate at 69% and 35% of the full capacity for an execution ratio of 1:5 and 1:10, respectively. For that reason, by reducing the sampling frequency of the main loop by 50%, an equivalent reduction of the computational resources on the DSP is achieved. From Figure 10, the relationship between the amplitude of the displacement $x(t)$ and relative error between the mrRTHS and reference is identified. Here, it appear that an increasing amplitude amplifies the error. When the external load ceases after approximately 55 sec cf. Figure 9, the freely oscillating system will gradually decay with a frequency equal to the modal period. However, due to actuator dynamics and communication delay, the damping of the mrRTHS is lower than the reference, causing the error to gradually magnify during the free oscillation period.



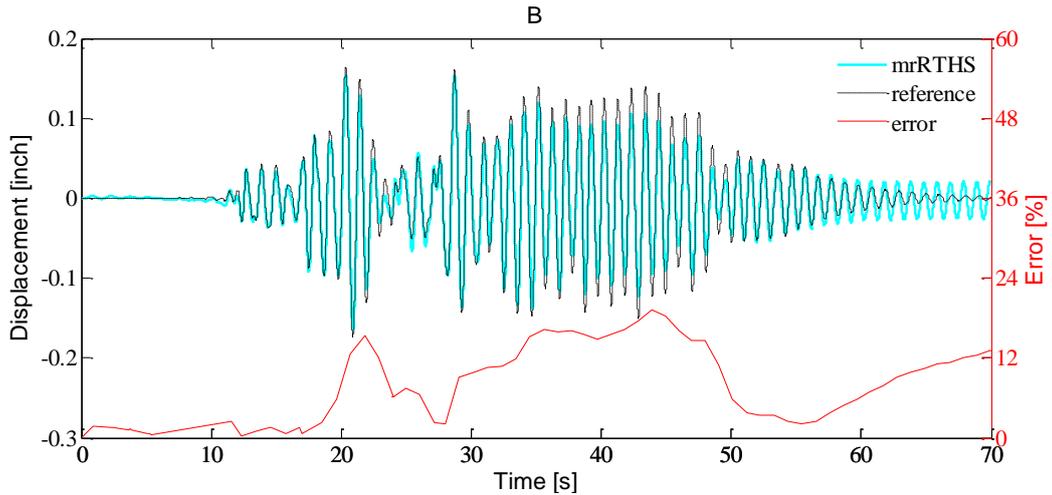


Figure 10: displacement response and error for the SDOF system with: a) execution ratio 1:5 and b) execution ratio 1:10

The corresponding actuator performance in the time domain for both execution ratios are presented in Figure 11. Here, a sound correlation between the desired and measured displacement of the actuator is identified, indicating that the single-order FF compensator is adequate for the given application.

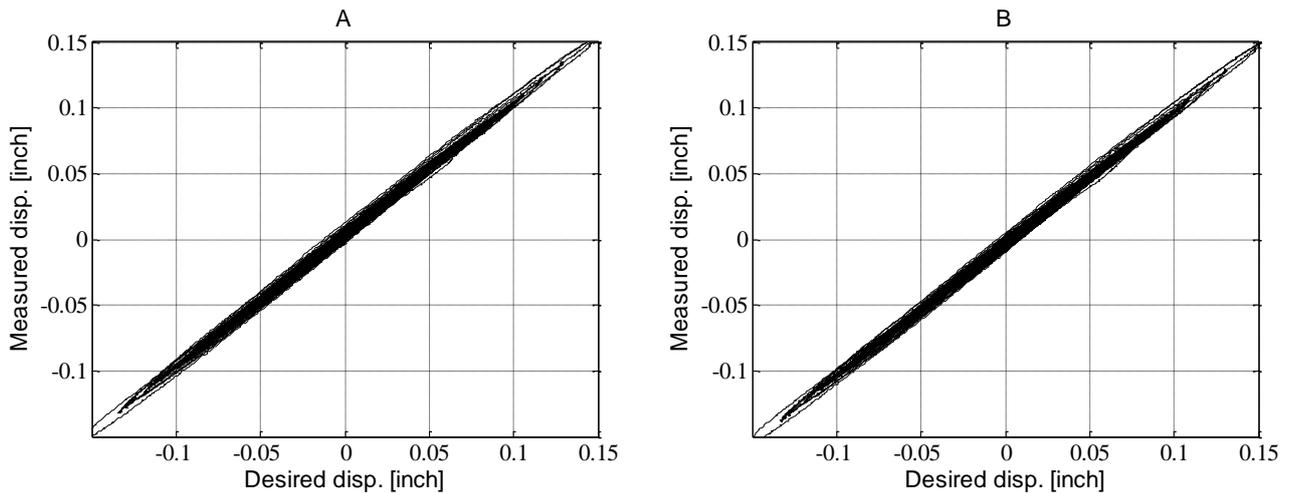


Figure 11: Time domain comparison of actuator performance with the single-order FF controller: A) execution ratio 1:5 and b) execution ratio 1:10

In Table 2, the RMS and peak error between the mrRTHS and reference are presented for execution ratios of 1:5 and 1:10. To isolate the error induced by the extrapolation algorithm through the communication delay compensator and extrapolation procedure, the experimental substructure is substituted by a numerical model – referred to here as numerical mrRTHS. With this modification, the experimental errors including transfer system dynamics, sensor miscalibration, measurement noise and random truncations in the analogue-to-digital (AD) conversion of the signal are eliminated.

Execution ratio [-]	mrRTHS RMS error [%]	Num. mrRTHS RMS error [%]	mrRTHS peak error [%]	Num. mrRTHS peak error [%]
5	7.45	1.10	20.64	3.21
10	7.67	1.15	21.82	3.33

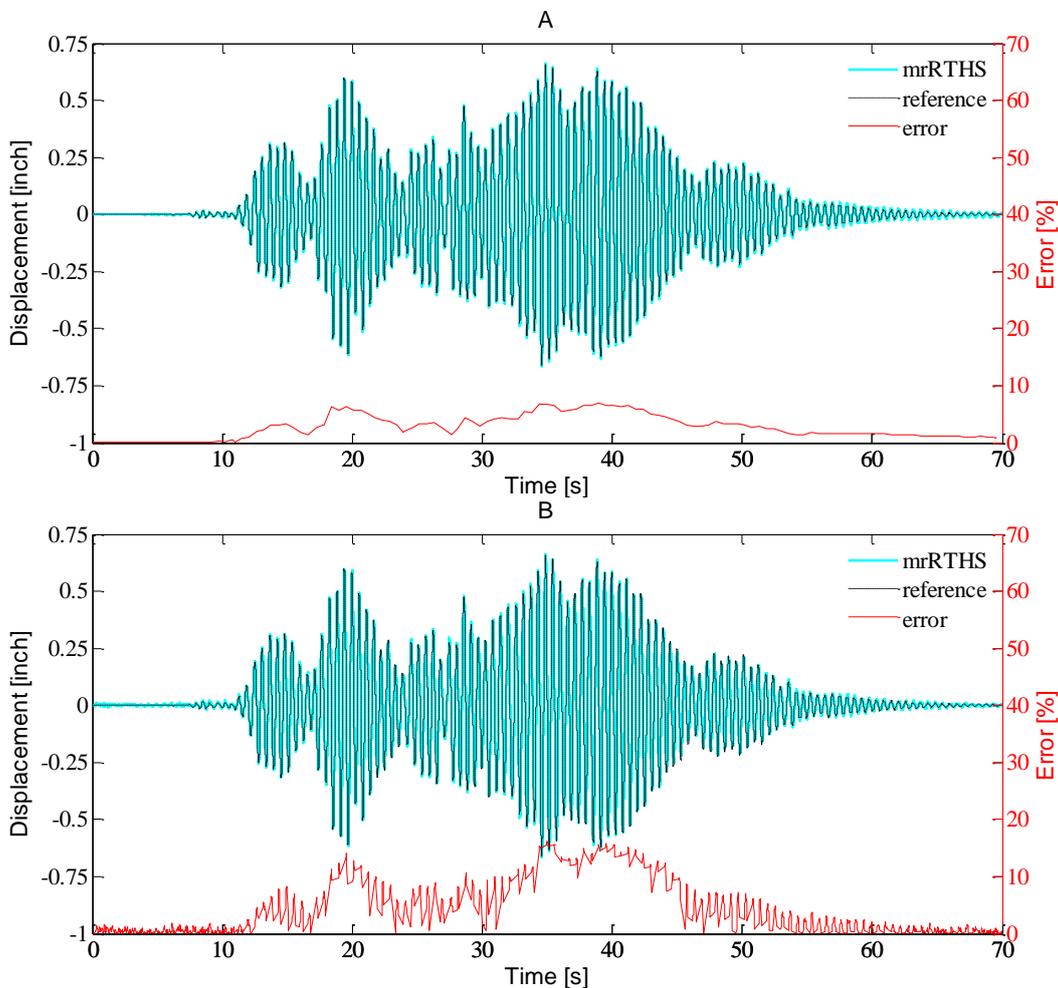
Table 2: RMS and peak error obtained through SDOF mrRTHS and numerical mrRTHS

From Table 2, approximately 15% of the RMS and peak error are generated by the extrapolation procedure for both execution ratios, meaning that other sources of errors – also present in conventional RTHS – comprise the remaining 85% of the total error. Furthermore, by increasing the execution ratio from 1:5 to 1:10, a 50% reduction of the

1 computational resources of the DSP is achieved, with the tradeoff of increasing the error between the mrRTHS and
2 reference by approximately 4%.
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4 5.2. MDOF mrRTHS

6 For the MDOF mass-spring-damper system, the displacement $x_3(t)$ relative to the ground (see Figure 7a) are presented
7 for the mrRTHS and reference for execution ratios of 1:5 and 1:10 in Figure 12. Note that the displacement of the
8 shared boundary - given by $x_3(t)-x_2(t)$ cf. Figure 7a - is on the same order as the displacement of the SDOF system. The
9 corresponding relatively error between the mrRTHS and reference are determined cf. eq. 10. The time step of the
10 primary operation of the main loop Δt_p is for the MDOF configuration 2ms due to the enhanced complexity of the
11 numerical substructure. Furthermore the work load of the DSP is 75% and 38% of the full capacity for execution ratios
12 of 1:5 and 1:10. For that reason, by reducing the frequency of the main loop by 50% an equivalent reduction of the
13 computational resources on the DSP is achieved. From Figure 12, the relation between the amplitude of the
14 displacement $x_3(t)$ and relatively error between the mrRTHS and reference is found to be identical to the SDOF system.
15 However, due to the increased magnitude of displacement, the error is reduced relative to the SDOF system cf. eq.
16 (10).
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54 Figure 12: displacement response and error for the MDOF system with: a) execution ratio 1:5 and b) execution ratio 1:10

55 The corresponding actuator performance in the time domain for both execution ratios are presented in Figure 13.
56 Here a sound correlation between the desired and measured displacement of the actuator is identified for an
57 execution ratio of 1:5, indicating that the third-order FF compensator is adequate for the given application. However
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when the execution ratio is increased to 1:10 some major inconsistencies between the desired and measured displacement is observed. This outcome is probably caused by the instability induced by the irregular step between the last extrapolated point $d_{exp}(t)$ and consecutive displacement signal $d_{pred}(t)$, see Figure 6b. This instability does likewise appear in the error represented in Figure 12b. In Table 3 the RMS and peak error between the mrRTHS and reference along with the numerical mrRTHS and reference are presented for execution ratios of 1:5 and 1:10.

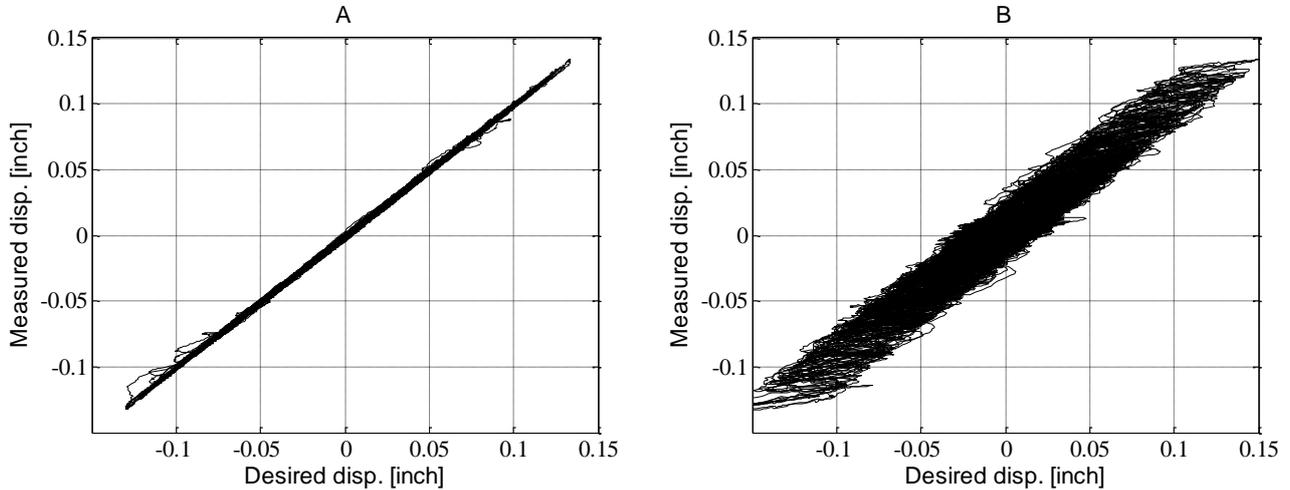


Figure 13: Time domain comparison of actuator performance with the third-order FF controller: A) execution ratio 1:5 and b) execution ratio 1:10

Execution ratio [-]	mrRTHS RMS error [%]	Num. mrRTHS RMS error [%]	mrRTHS peak error [%]	Num. mrRTHS peak error [%]
5	2.50	0.70	7.14	2.07
10	5.41	1.77	16.05	5.12

Table 3: RMS and peak error obtained through MDOF mrRTHS and numerical mrRTHS

From Table 3, approximately 30% of the RMS and peak error is generated by the extrapolation procedure for both execution ratios, meaning that other sources of error – also present in conventional RTHS – comprise the remaining 70% of the total error. It is noted that this error is identified to be 15% for the SDOF system. However due to the increase in frequency, the error induced by the extrapolation procedure will increase cf. Figure 6a. When the execution ratio is increased from 1:5 to 1:10, a 50% reduction of the computational resources is achieved; however this comes with a 60% increase in the error between the mrRTHS and reference. Compared with the SDOF system, this is a significant increase in the error induced by the extrapolation procedure. A reduction of this error could be achieved by using a different or higher order polynomial fitting extrapolator.

6. Discussion

The polynomial fitting extrapolator is implemented to handle both the communication delay and extrapolation procedure in the main loop. This algorithm consumes very little computational resources, making it suitable for real time hybrid simulation, especially for low-cost execution. However, for an increasing execution ratio and/or sampling frequency, the error induced by the polynomial fitting extrapolator leads to a reduced correlation between the mrRTHS and reference cf. Figure 6a. Increasing the order of the polynomial fitting extrapolator enables the algorithm to handle higher frequencies; however, that comes with an enhanced vulnerability to system noise and required computation resources. Other applicable extrapolation algorithms exists including least-square polynomial fitting, linearly predicted acceleration scheme and multi-rate linear compensation cf. [24]. From [24] the performance of the least-square polynomial fitting is found identical to the polynomial fitting extrapolator while the linearly predicted acceleration scheme only exhibits improved performance for an execution ratio below 1:5. The multi-rate linear compensator provides significantly better performance relative to the polynomial fitting extrapolator for both

1 execution ratios of interest; however this performance comes with the cost of significantly higher computational
2 resources.
3

4 Between each data point provided by the numerical substructure, a finer displacement signal is generated through
5 extrapolation. This approach provides a relatively short communication delay equivalent to the duration of the
6 primary operations on the DSP Δt_p which is 1-2ms in the applied case. Other publications concerning mrRTHS combine
7 extrapolation/interpolation to generate the displacement signal handled in the outer loop cf. [8], [22] and [23].
8 Through this method, extrapolation is performed until the numerical model is computed and the next displacement
9 signal identified – which is equivalent to the duration of Δt_p in the applied case. The remaining portion of the finer
10 displacement signal, equivalent to the duration of Δt_s in the applied case, is generated by interpolation. The
11 communication delay is for that reason given by the time step of the main loop, which in the applied case is 10ms.
12 Pure extrapolation provides for that reason a reduced communication delay relative to the combined
13 extrapolation/interpolation procedure. However, given that the error is gradually increasing during each
14 extrapolation sequence cf. Figure 6b, and an irregular step is bound between the last extrapolated point and
15 consecutive displacement signal; a limited number of extrapolation points would be preferable.
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20 To ensure continuous real-time loading of the shared boundary, displacement signals must be available in the outer-
21 loop at all times. For the applied configuration of the main- and outer-loop switching logic, the number of
22 extrapolated points is deemed consistent throughout the entire duration of the mrRTHS. For that reason, only explicit
23 numerical models which exhibit a consistent and predictable integration time can be handled in this configuration to
24 satisfy the explicit deadlines in the switching logic between the main- and outer-loop. To allow implicit numerical
25 models, the number of extrapolated points has to vary depending on the current integration time. This could be
26 achieved by making an estimate of the number of extrapolated points, followed by either erasing or adding additional
27 extrapolated points if the integration time of the numerical model is shorter or longer than estimated.
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31 **7. Conclusion**

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33 An mrRTHS configuration was implemented on a LabVIEW real-time target model: cRIO – 9074, capable of operating
34 the numerical and experimental substructure at two different rates to optimize computational resources while
35 maintaining good actuator control. The system proved that by reducing the execution rate of the numerical
36 substructure by 50% an equivalent reduction of the computational resources on the DSP were achieved. This proves
37 the mrRTHS configuration as an effective method in optimizing the computational resources, extending the
38 capabilities of existing RTHS systems.
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41 The mrRTHS was demonstrated through an SDOF and MDOF mass-spring-damping system and the performance
42 evaluated against the corresponding reference. For the SDOF configuration relative RMS errors of 7.45% and 7.67%
43 were identified between the mrRTHS and reference for an execution ratio of 1:5 and 1:10, respectively. The same RMS
44 errors were identified to 2.50% and 5.41% for the MDOF configuration. Due to the magnification of the amplitude for
45 the MDOF configuration relative to the SDOF system, a reduction of the RMS error was identified. By reducing the
46 frequency of the main loop with 50% an equivalent reduction of the computational resources on the DSP were
47 achieved. These savings in computational resources came with the tradeoff of a 4% and 60% increase in the error
48 between the mrRTHS and reference for the SDOF and MDOF configurations, respectively.
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52 The error induced by the polynomial fitting extrapolator was found to include an irregular step between the last
53 extrapolated point and consecutive displacement signal. This discontinuity introduced some chattering in the system
54 which became distinct for the MDOF system with an execution ratio of 1:10. To isolate the error induced by the
55 polynomial fitting extrapolator operated in the main loop, the experimental substructure was replaced by the
56 numerical model. From this analysis, it was found that 85% and 70% of the RMS error between the mrRTHS and
57 reference were generated by other experimental errors for the SDOF and MDOF configuration, respectively. This
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1 indicates that other sources of error including: transfer system dynamics, sensor miscalibration, measurement noise
2 and random truncations in the analogue-to-digital (AD) conversion, which likewise appear in conventional RTHS, are
3 attributed for the majority of the error between the mrRTHS and reference.
4

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6
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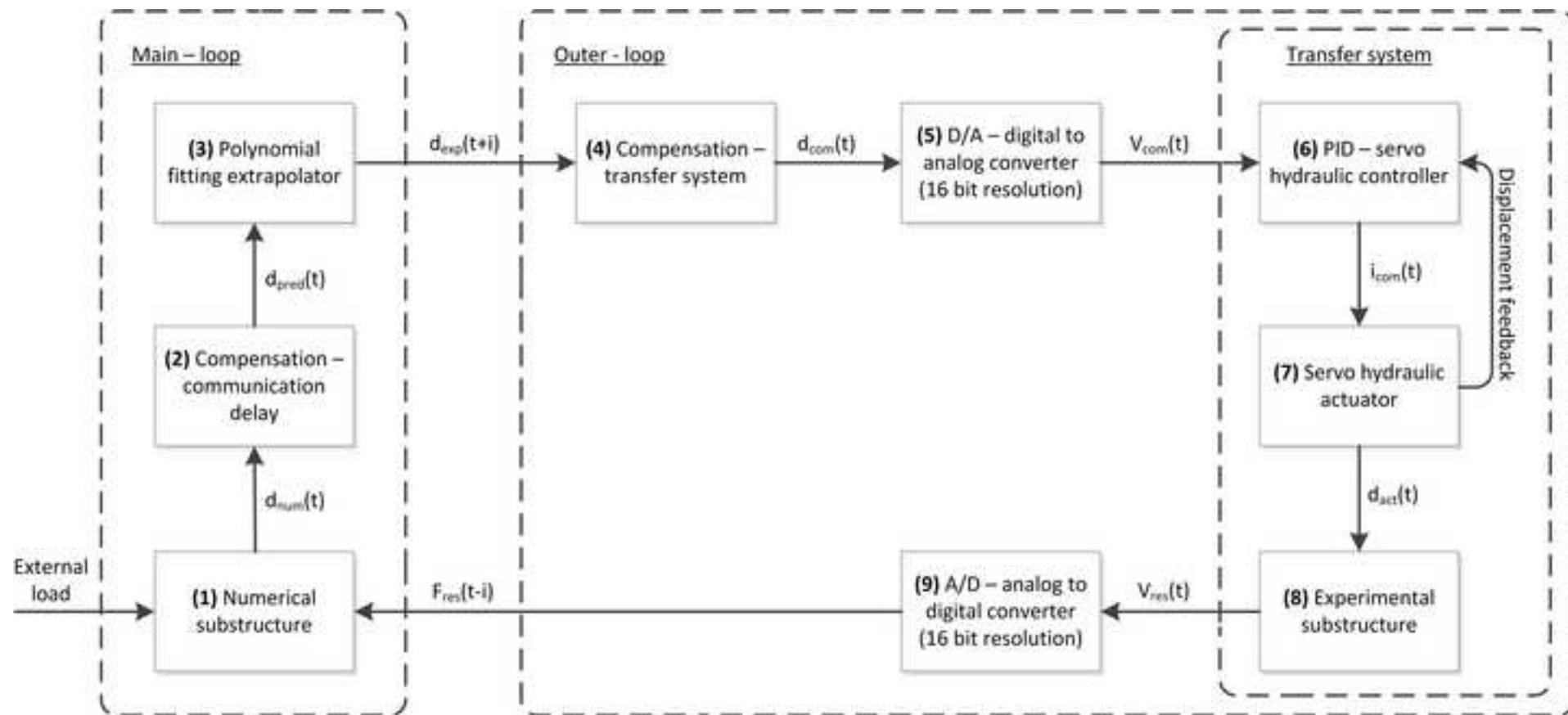
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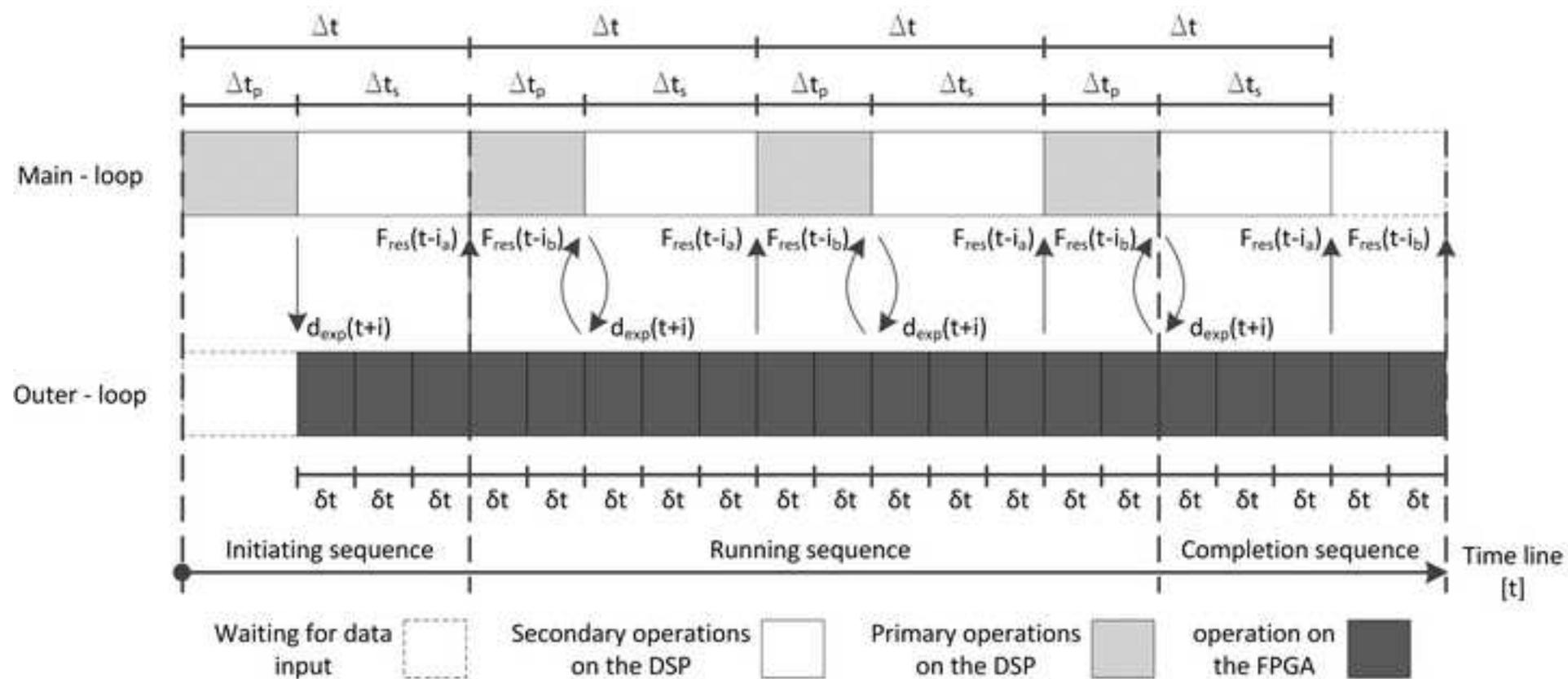
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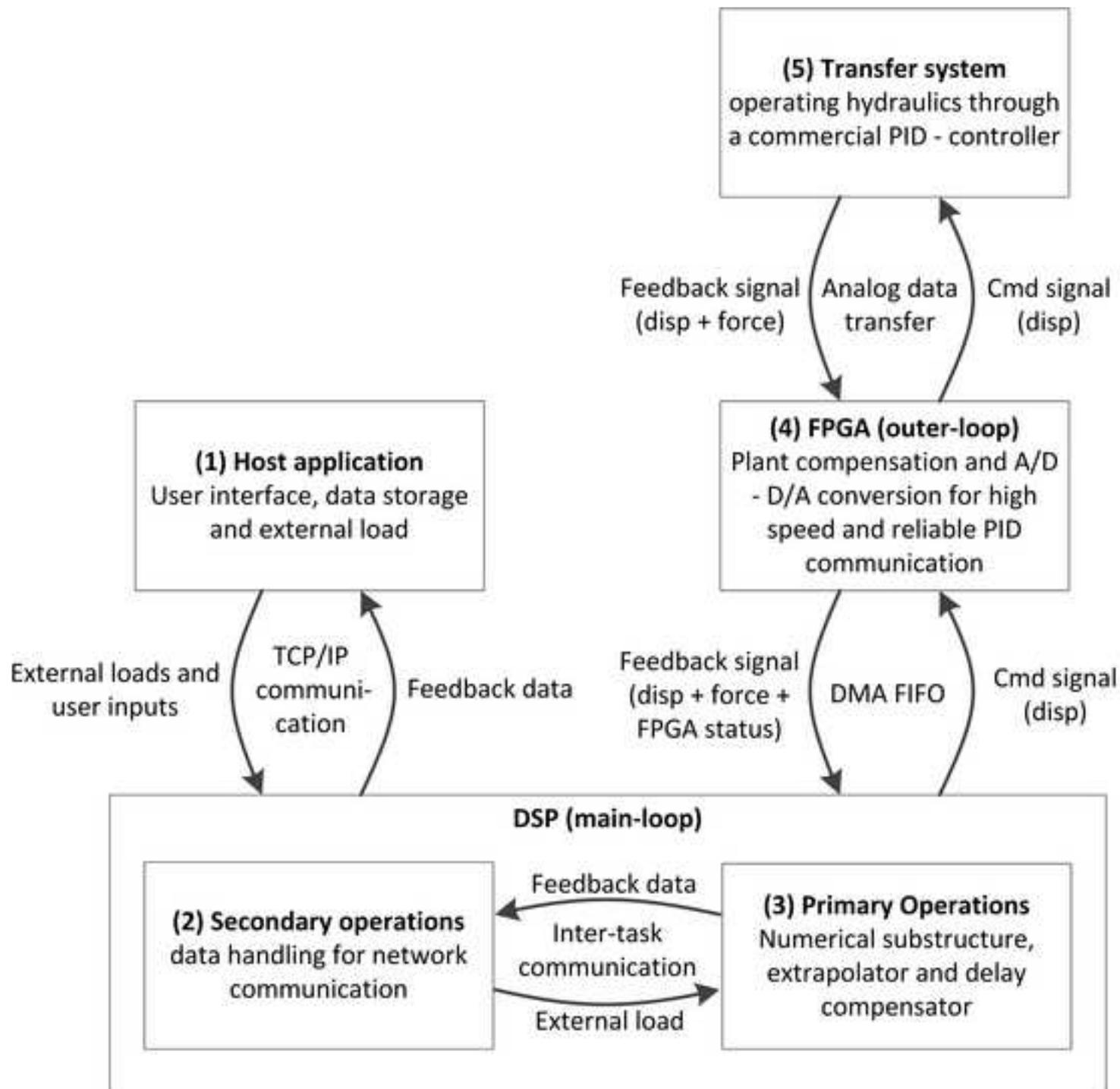
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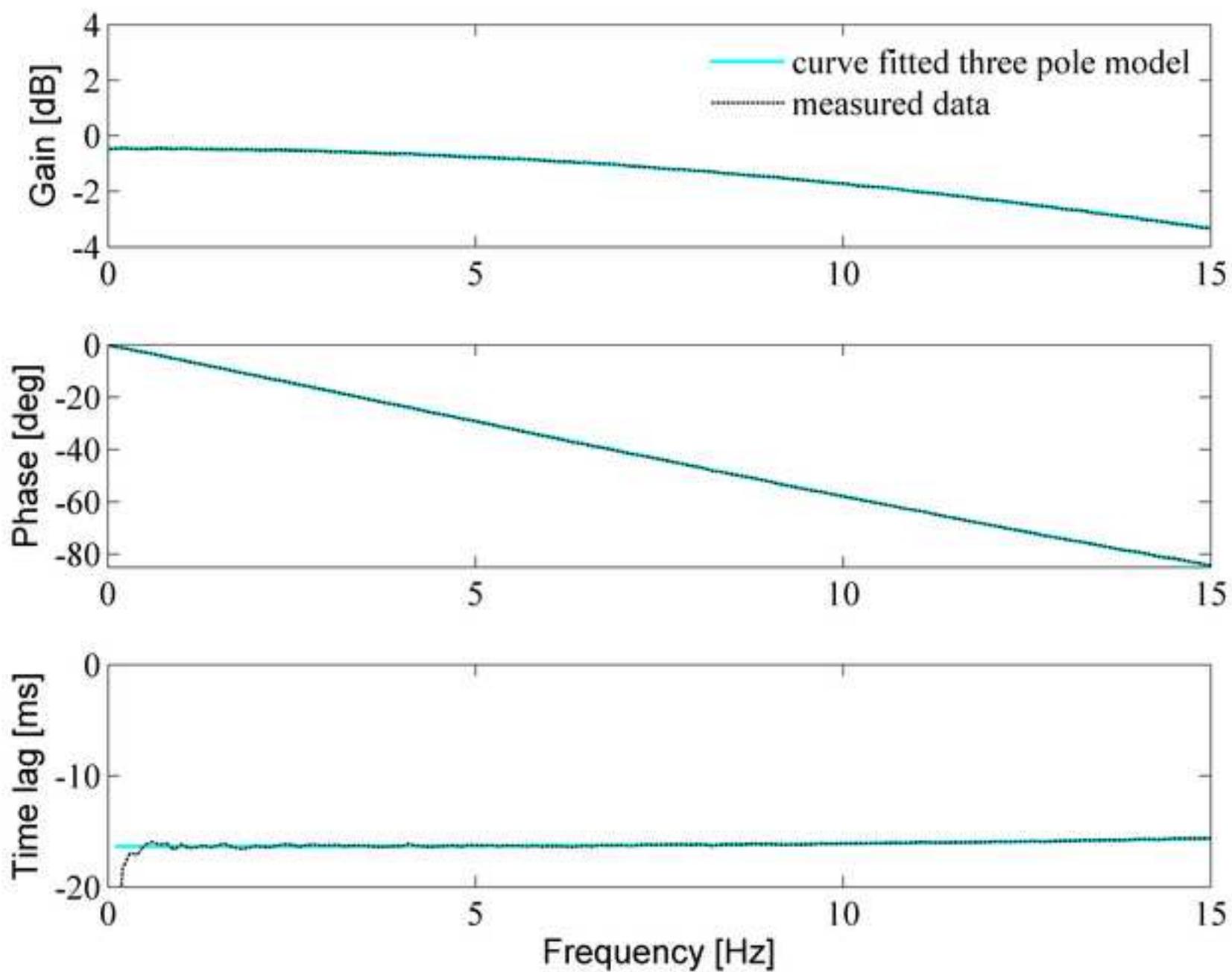
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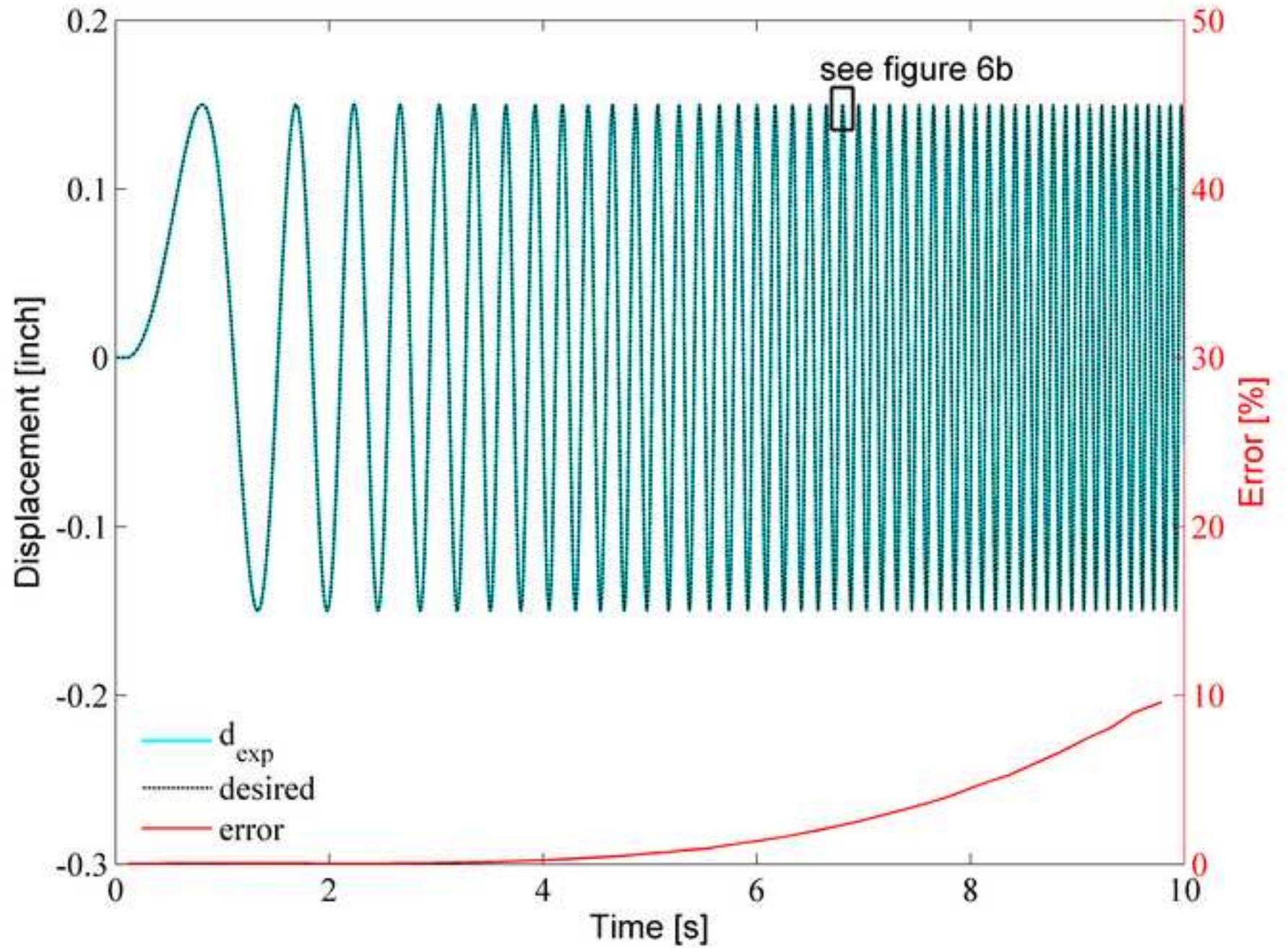


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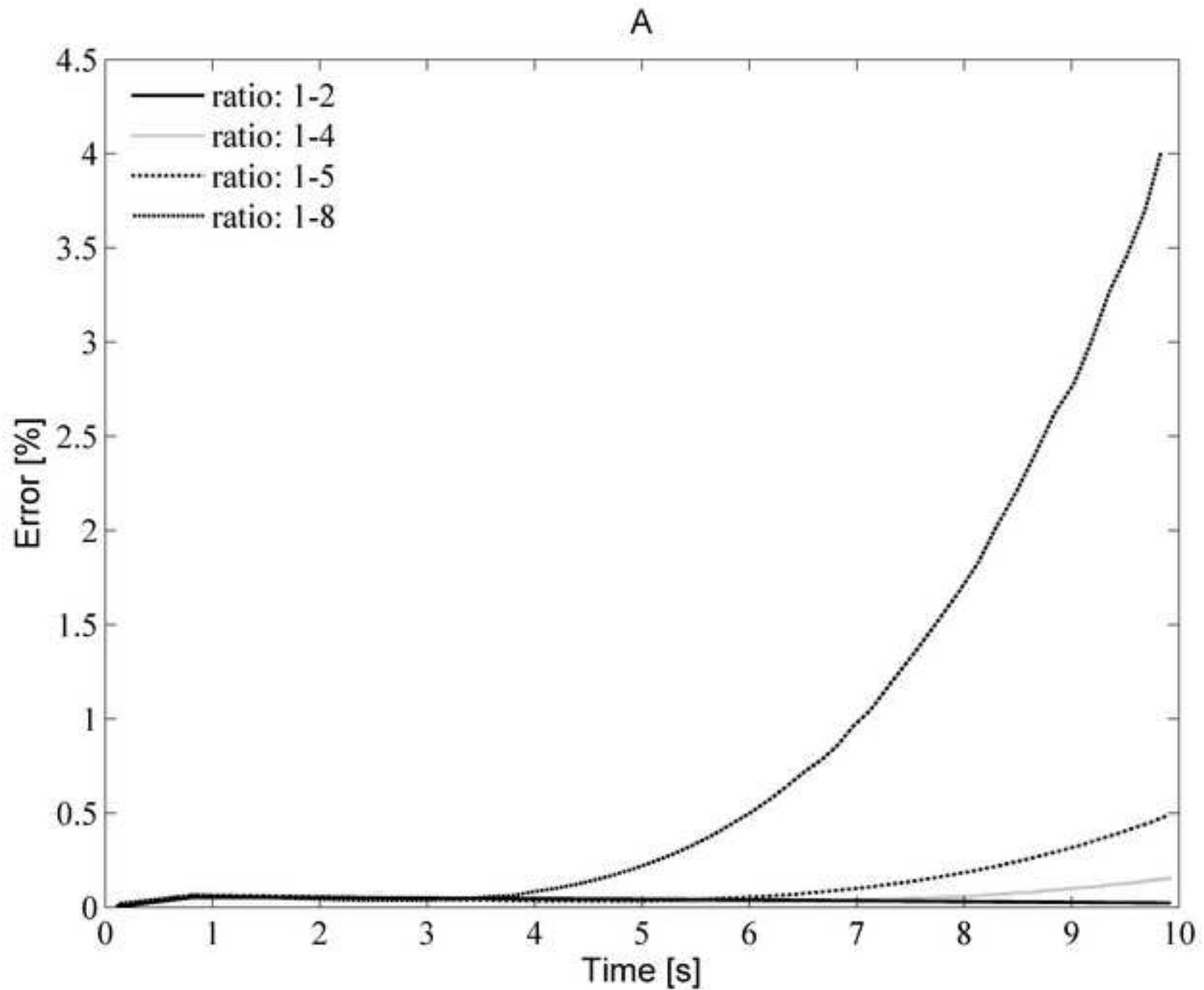
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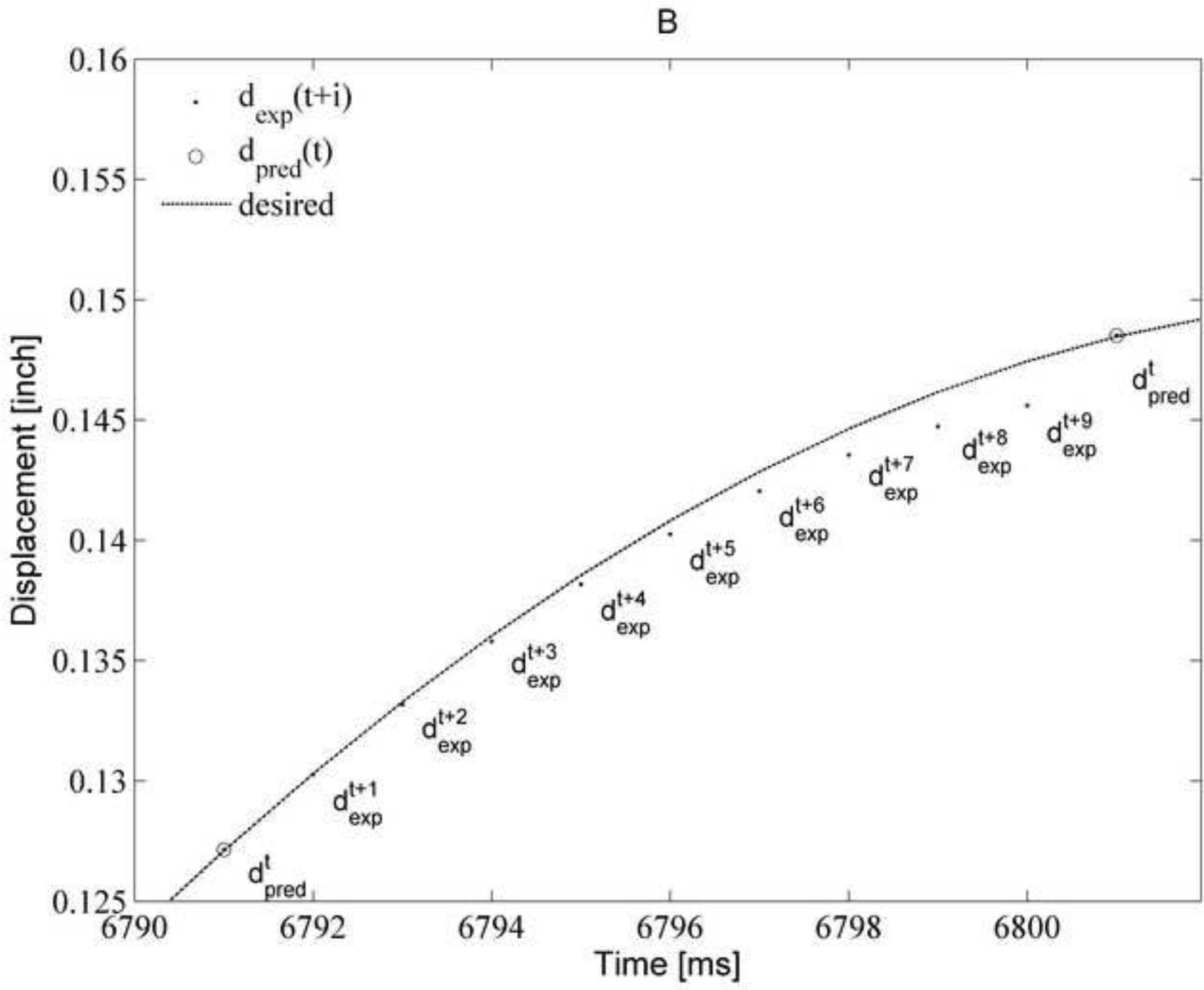
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Figure_6a
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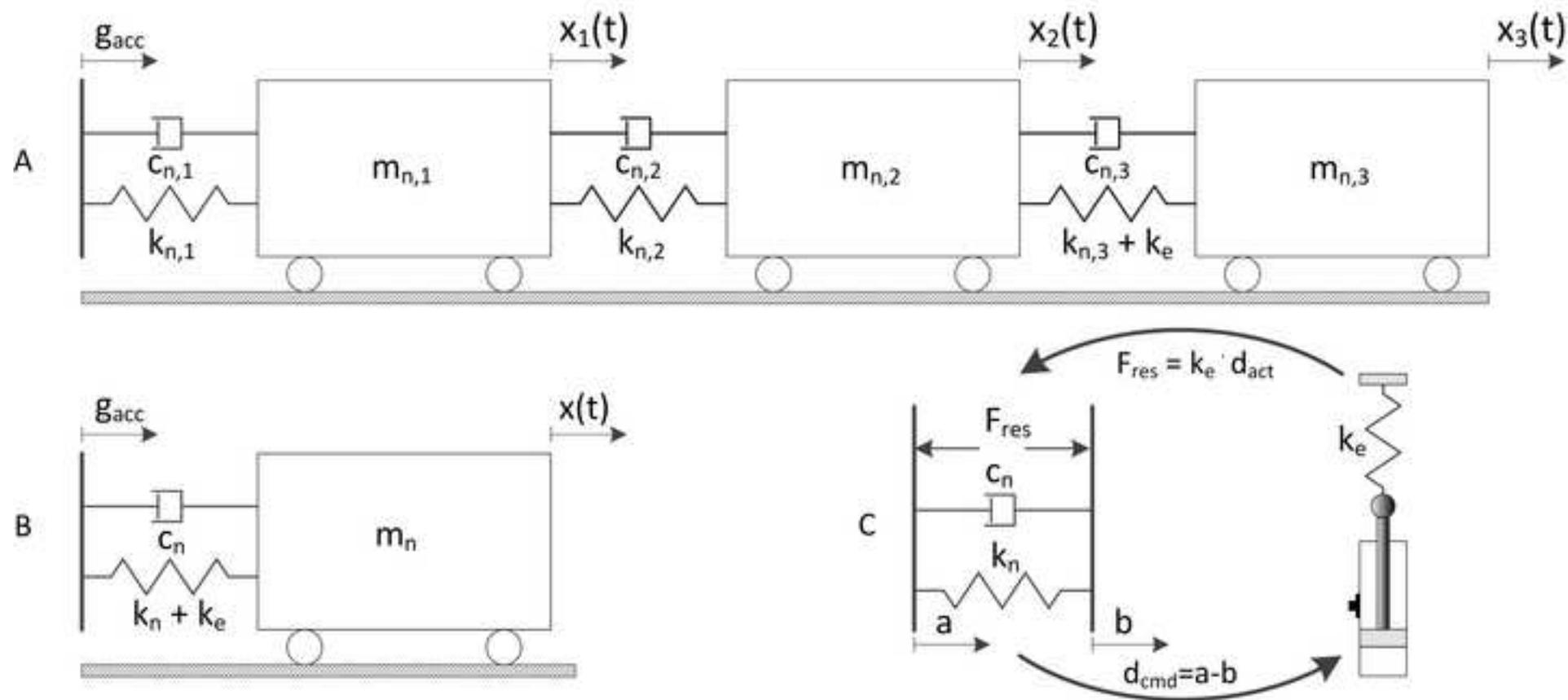


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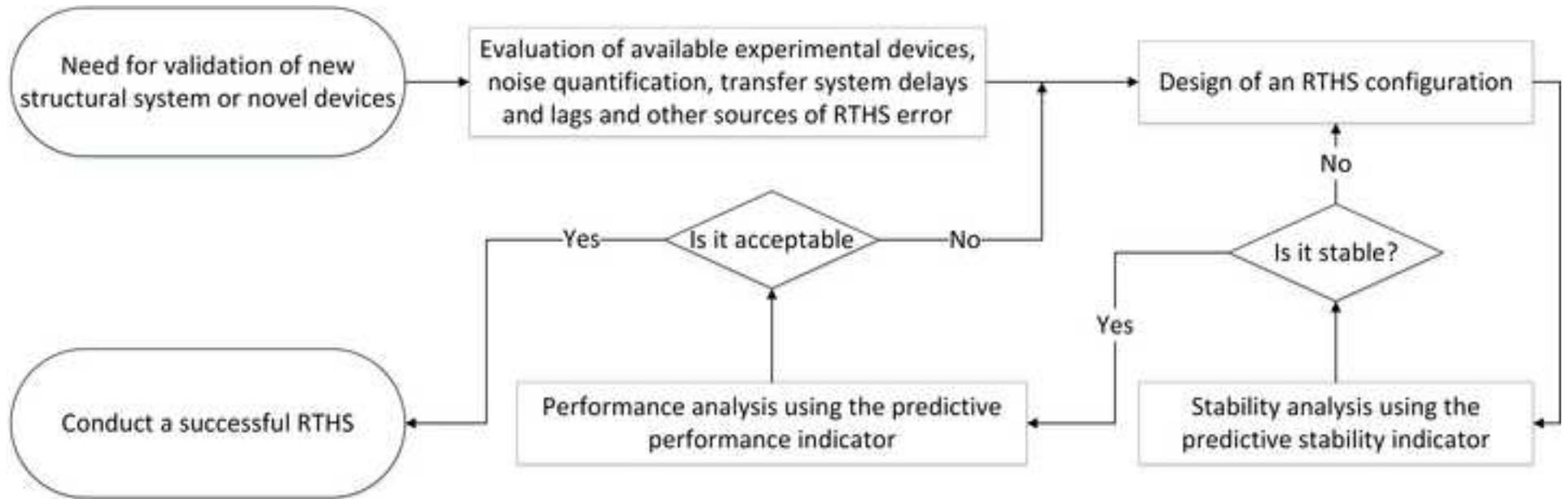


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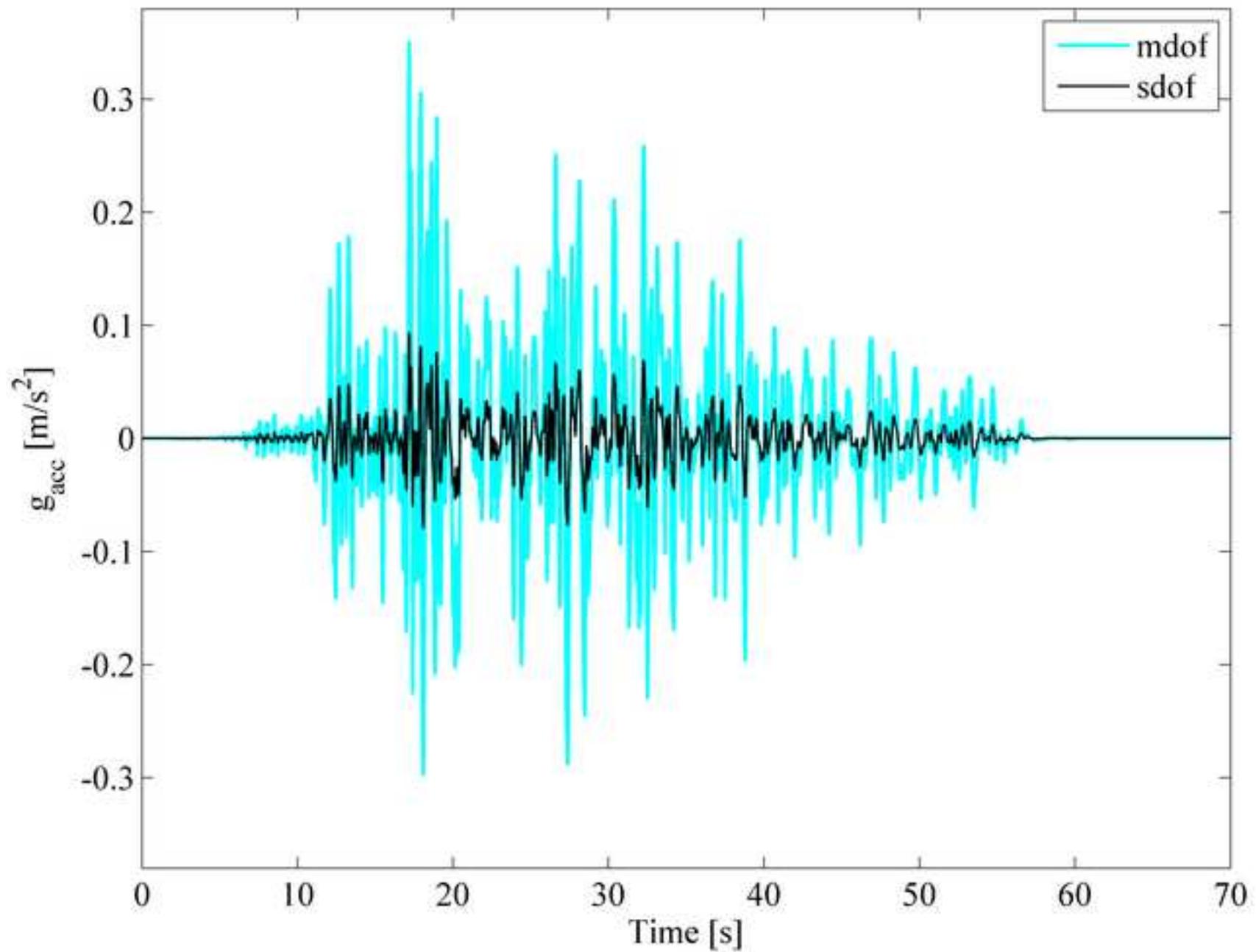
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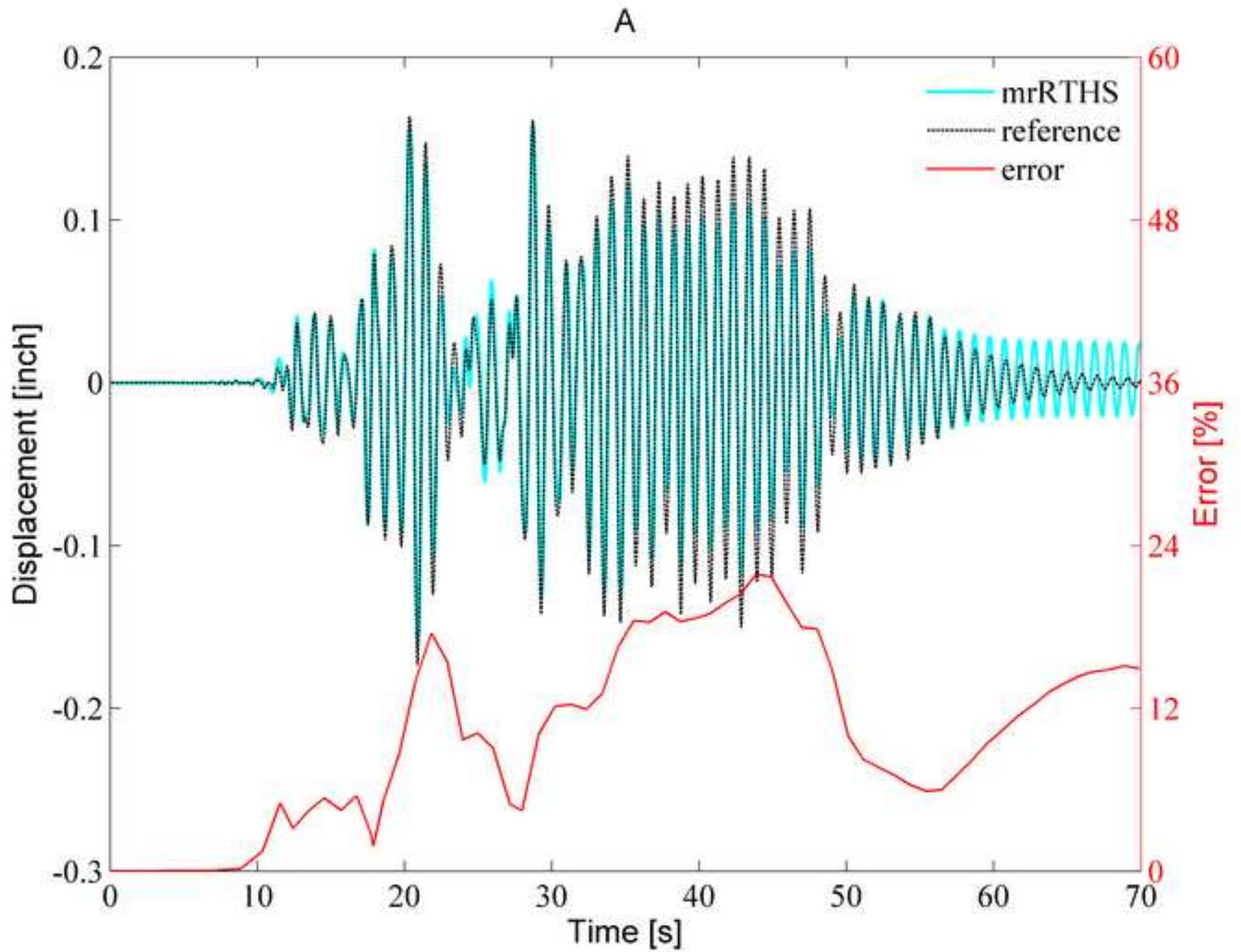
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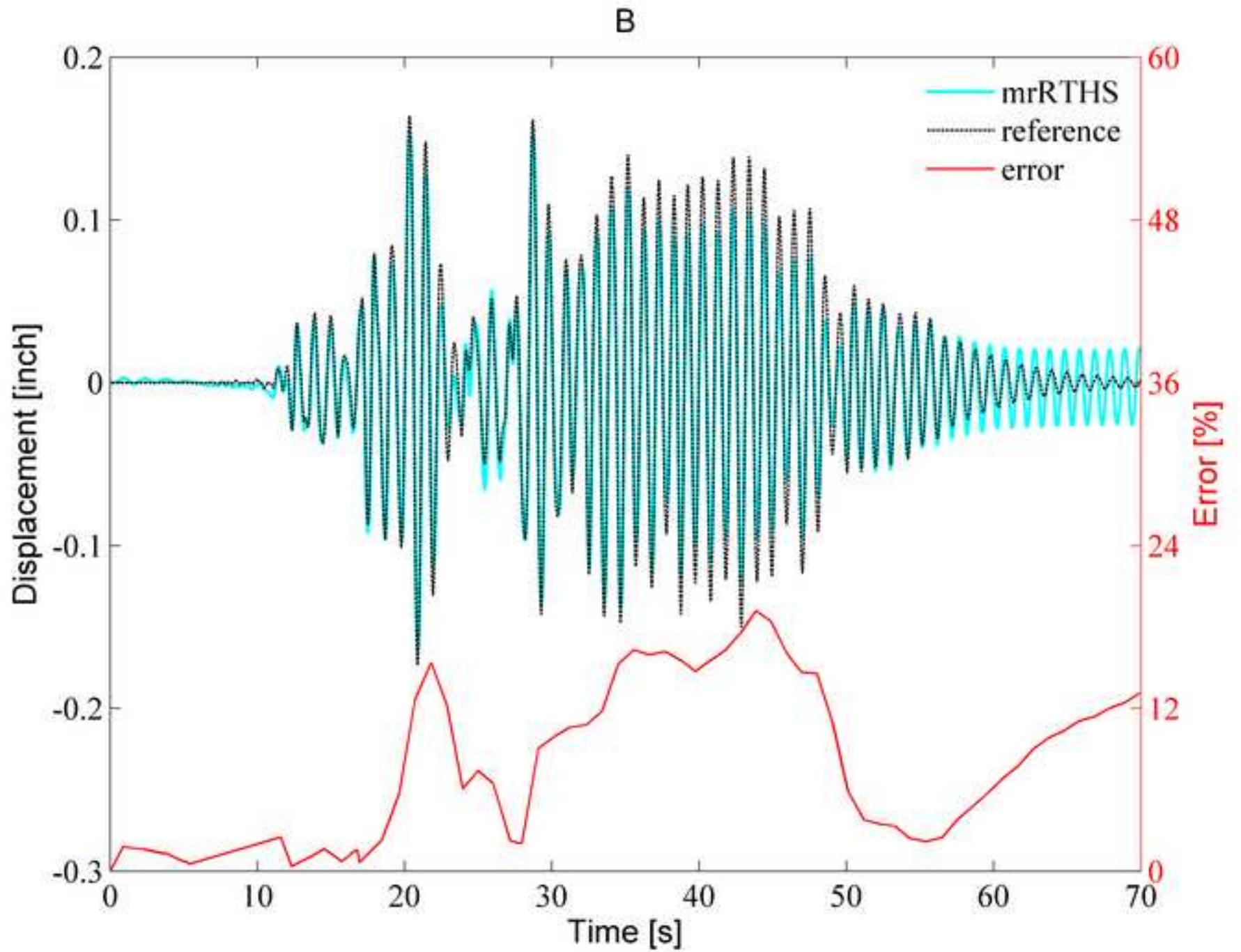
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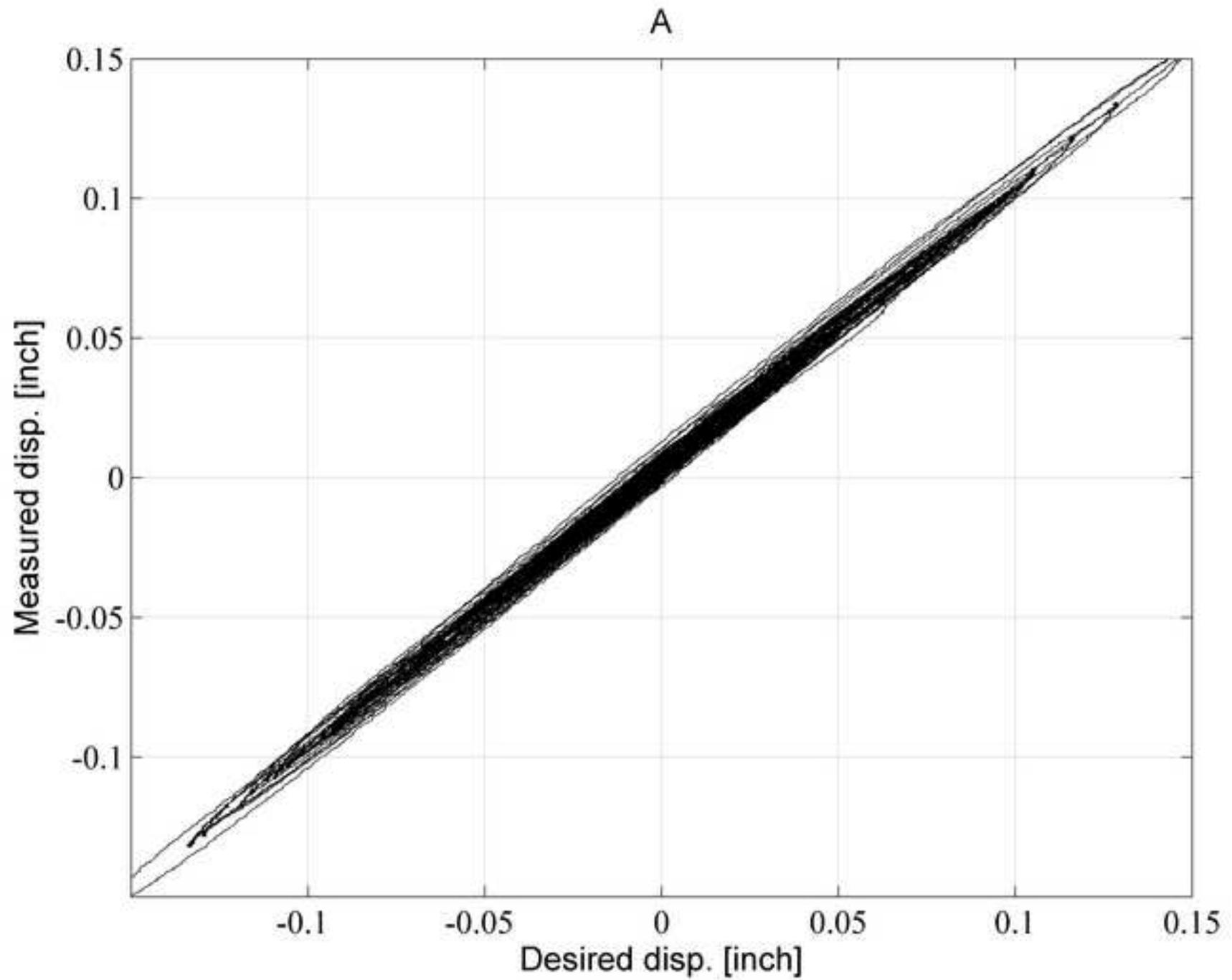
Figure_10a
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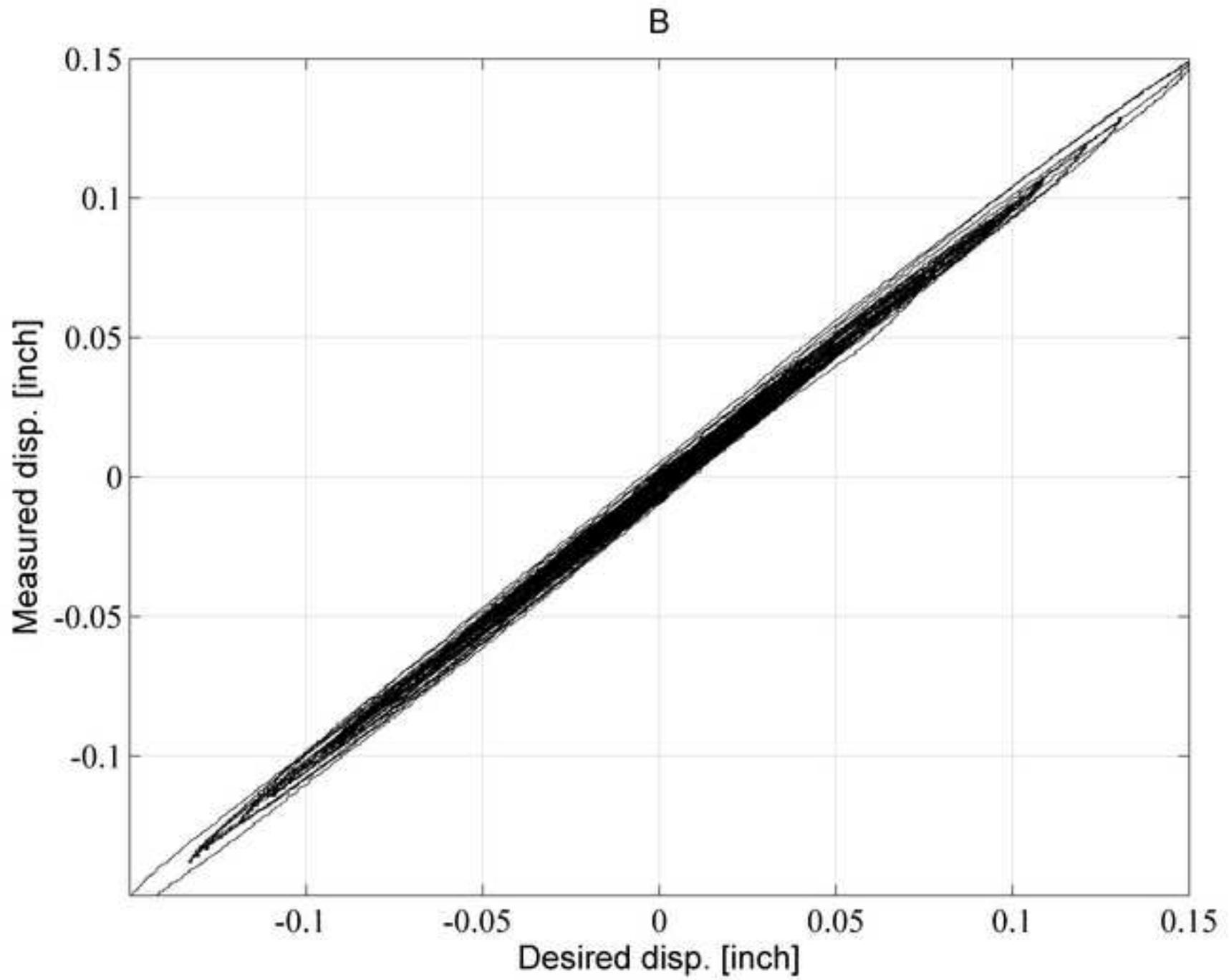
Figure_10b
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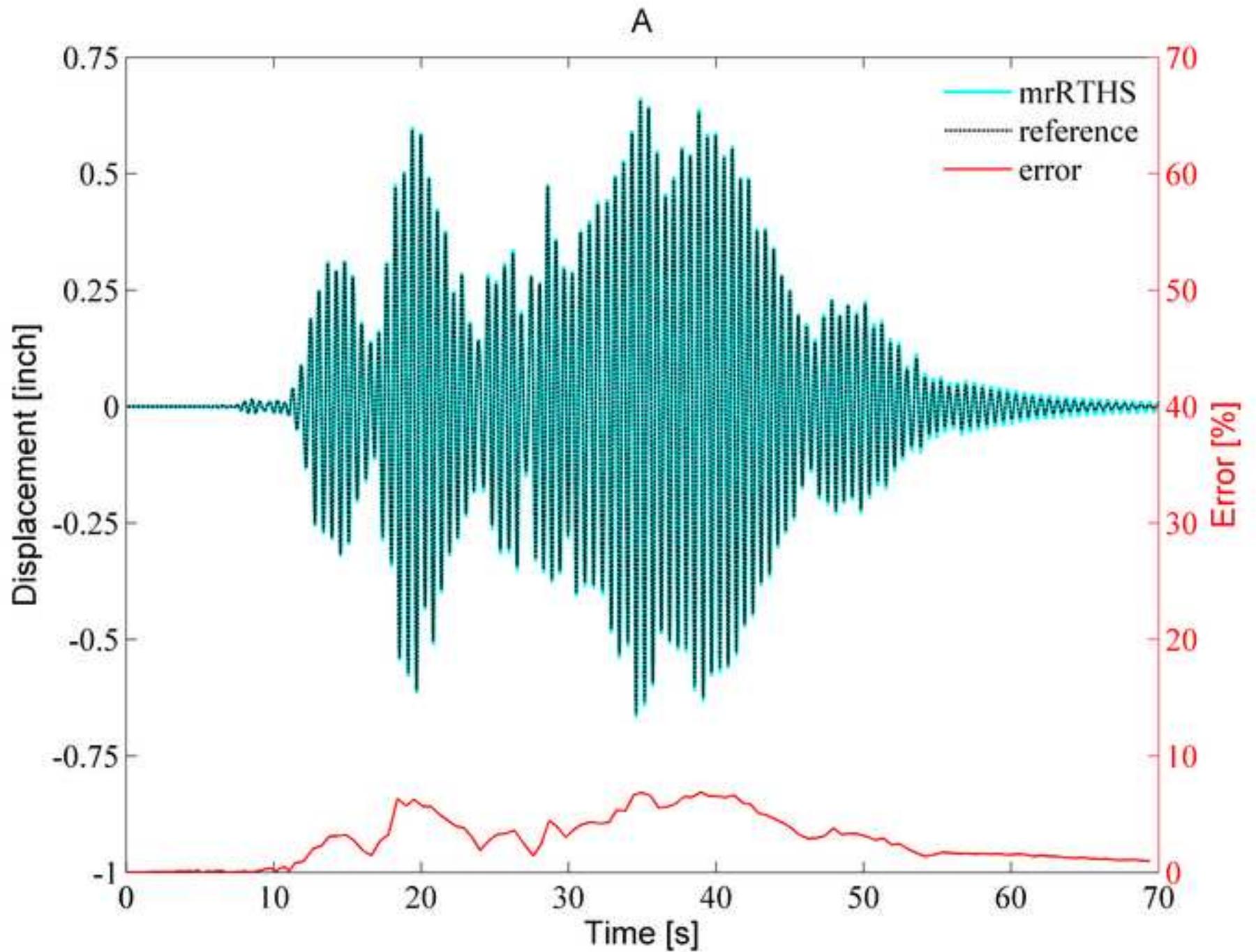
Figure_11a
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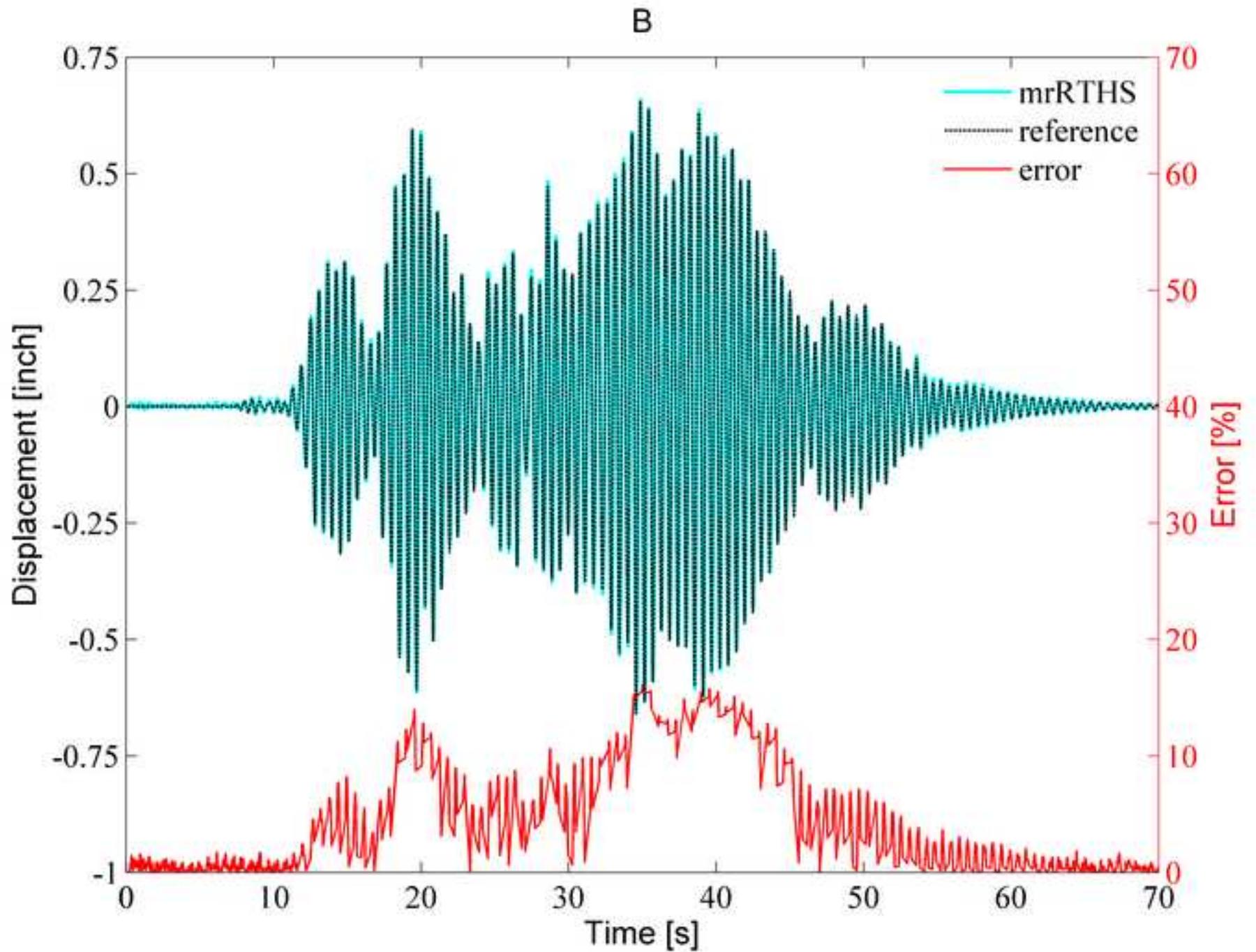
Figure_11b
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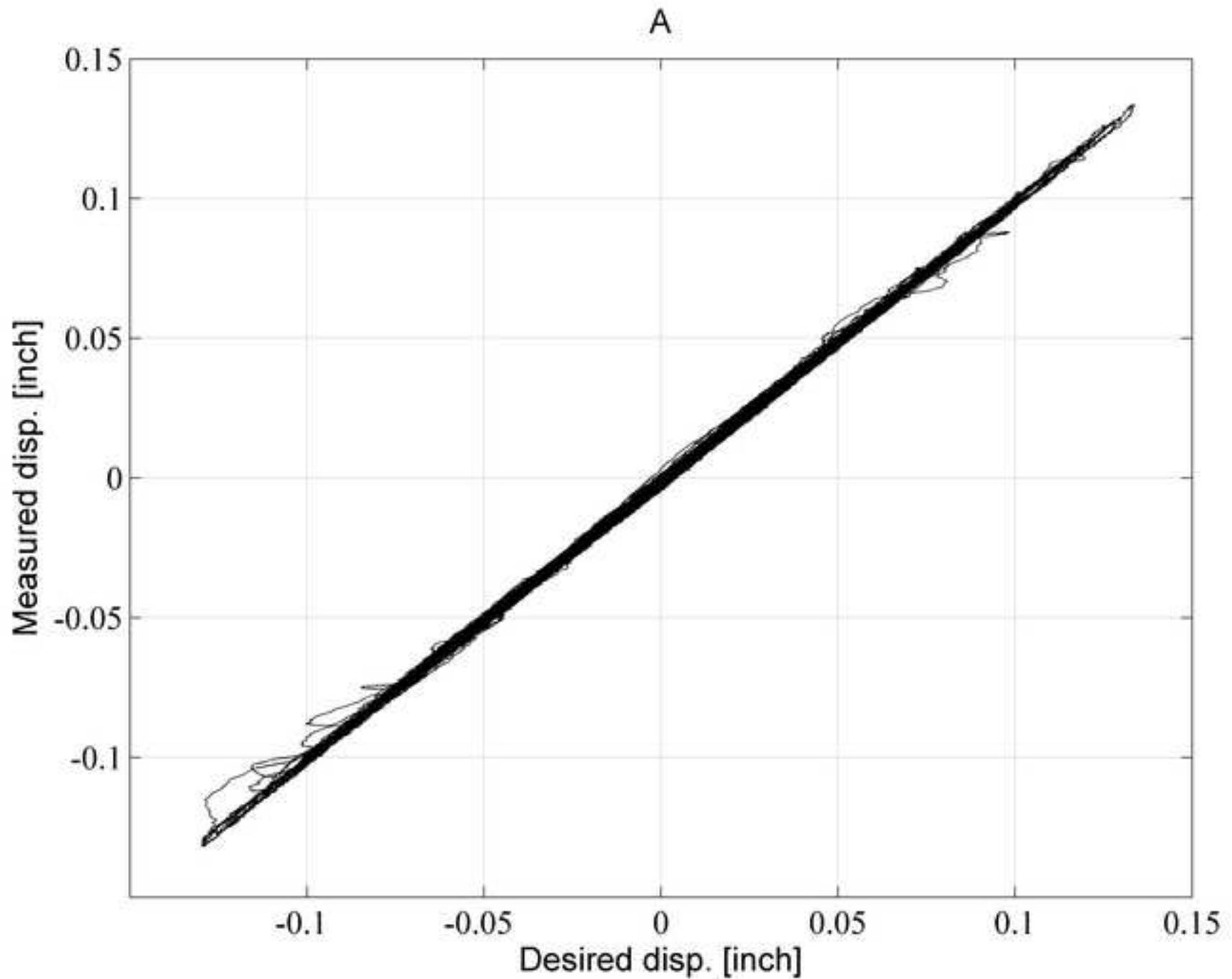
Figure_12a
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Figure_12b
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Figure_13a
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Figure_13b
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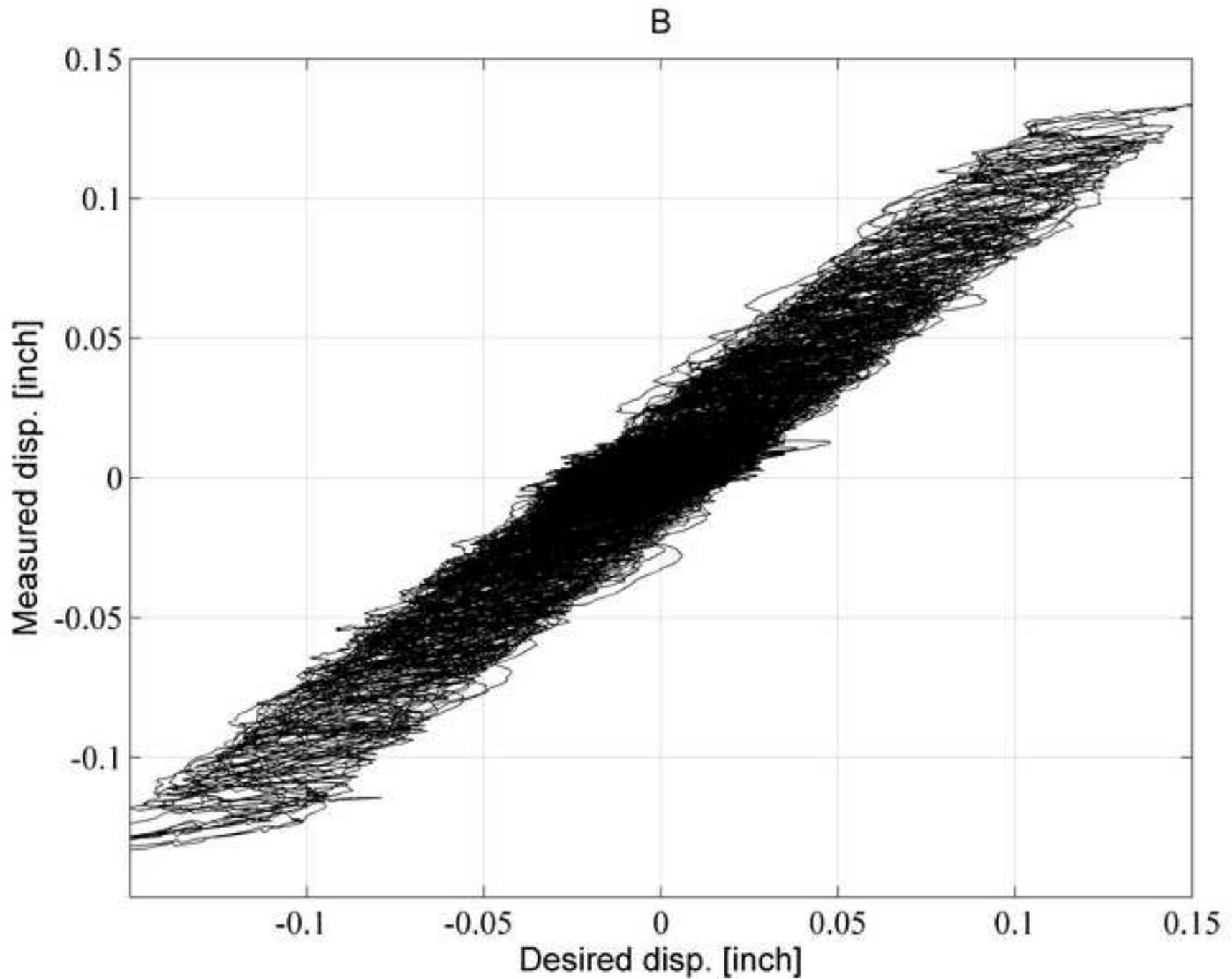


Figure 4 - Supplementary MATLAB .fig files

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Figure 5 - Supplementary MATLAB .fig files

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Figure 6a - Supplementary MATLAB .fig files

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Figure 6b - Supplementary MATLAB .fig files

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Figure 9 - Supplementary MATLAB .fig files

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Figure 10a - Supplementary MATLAB .fig files

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Figure 10b - Supplementary MATLAB .fig files

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Figure 11a - Supplementary MATLAB .fig files

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Figure 12a - Supplementary MATLAB .fig files

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